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EIN No: SSDCM6-065 Rev. A Date: January 12, 2024 Originator: Enterprise SSD Product Group 1

Engineering Information Notice (EIN)

PRODUCT AFFECTED

For Generic, Std, KCM6 series

KCM61RULxxxx Series: 1 DWPD
- KCM61RUL960G: SDFHS06GEAxxx
- KCM61RUL1T92: SDFHS05GEAxxx
- KCM61RUL3T84: SDFHS04GEAxxx
- KCM61RUL7T68: SDFHS03GEAxxx
- KCM61RUL15T3: SDFHS01GEAxxx
- KCM61RUL30T7: SDFHS00GEAxxx

KCM61VULxxxx Series: 3 DWPD
- KCM61VUL800G: SDFHQ06GEAxxx
- KCM61VUL1T60: SDFHQ05GEAxxx
- KCM61VUL3T20: SDFHQ04GEAxxx
- KCM61VUL6T40: SDFHQ03GEAxxx
- KCM61VUL12T8: SDFHQ01GEAxxx

For Generic, SIE, KCM6 series

KCM6XRULxxxx Series: 1 DWPD
- KCM6XRUL960G: SDFHS86GEBxxx
- KCM6XRUL1T92: SDFHS85GEBxxx
- KCM6XRUL3T84: SDFHS84GEBxxx
- KCM6XRUL7T68: SDFHS83GEBxxx
- KCM6XRUL15T3: SDFHS81GEBxxx
- KCM6XRUL30T7: SDFHS80GEBxxx

KCM6XVULxxxx Series: 3 DWPD
- KCM6XVUL800G: SDFHQ86GEBxxx
- KCM6XVUL1T60: SDFHQ85GEBxxx
- KCM6XVUL3T20: SDFHQ84GEBxxx
- KCM6XVUL6T40: SDFHQ83GEBxxx
- KCM6XVUL12T8: SDFHQ81GEBxxx

For Generic, SED, KCM6 series

KCM6DRULxxxx Series: 1 DWPD
- KCM6DRUL960G: SDFHS46GEBxxx
- KCM6DRUL1T92: SDFHS45GEBxxx
- KCM6DRUL3T84: SDFHS44GEBxxx
- KCM6DRUL7T68: SDFHS43GEBxxx
- KCM6DRUL15T3: SDFHS41GEBxxx
- KCM6DRUL30T7: SDFHS40GEBxxx

KCM6DVULxxxx Series: 3 DWPD
- KCM6DVUL800G: SDFHQ46GEBxxx
- KCM6DVUL1T60: SDFHQ45GEBxxx
- KCM6DVUL3T20: SDFHQ44GEBxxx
- KCM6DVUL6T40: SDFHQ43GEBxxx
- KCM6DVUL12T8: SDFHQ41GEBxxx

For Generic, FIPS, KCM6 series

KCM6FRULxxxx Series: 1 DWPD
- KCM6FRUL960G: SDFHS66GEBxxx
- KCM6FRUL1T92: SDFHS65GEBxxx
- KCM6FRUL3T84: SDFHS64GEBxxx
- KCM6FRUL7T68: SDFHS63GEBxxx
- KCM6FRUL15T3: SDFHS61GEBxxx
- KCM6FRUL30T7: SDFHS60GEBxxx

KCM6FVULxxxx Series: 3 DWPD
- KCM6FVUL800G: SDFHQ66GEBxxx
- KCM6FVUL1T60: SDFHQ65GEBxxx
- KCM6FVUL3T20: SDFHQ64GEBxxx
- KCM6FVUL6T40: SDFHQ63GEBxxx
- KCM6FVUL12T8: SDFHQ61GEBxxx

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CLASSIFICATION

[☐] Electrical
[☐] Mechanical
[☒] Others

LEVEL

[☐]Hardware
[☒] Software (firmware)
[☐] Document
[☐] Manufacturing
[☐] Others

IMPLEMENTATION

[☒] Factory
[☐] Customer side
[☐] As required
[☐] Repaired
[☐] Retrofit kit required

PRIORITY

[☐] Urgent
[☐] Immediate
[☒] Routine

REVISION LEVEL

For Generic, Std, KCM6 series

KCM61RULxxxx Series: 1 DWPD

KCM61RUL960G: SDFHS06GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61RUL1T92: SDFHS05GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61RUL3T84: SDFHS04GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61RUL7T68: SDFHS03GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61RUL15T3: SDFHS01GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM61RUL30T7: SDFHS00GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM61VULxxxx Series: 3 DWPD

KCM61VUL800G: SDFHQ06GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61VUL1T60: SDFHQ05GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61VUL3T20: SDFHQ04GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61VUL6T40: SDFHQ03GEAxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM61VUL12T8: SDFHQ01GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

For Generic, SIE, KCM6 series

KCM6XRULxxxx Series: 1 DWPD

KCM6XRUL960G: SDFHS86GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XRUL1T92: SDFHS85GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XRUL3T84: SDFHS84GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XRUL7T68: SDFHS83GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XRUL15T3: SDFHS81GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6XRUL30T7: SDFHS80GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6XVULxxxx Series: 3 DWPD

KCM6XVUL800G: SDFHQ86GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XVUL1T60: SDFHQ85GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XVUL3T20: SDFHQ84GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XVUL6T40: SDFHQ83GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6XVUL12T8: SDFHQ81GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

For Generic, SED, KCM6 series

KCM6DRULxxxx Series: 1 DWPD

KCM6DRUL960G: SDFHS46GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DRUL1T92: SDFHS45GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DRUL3T84: SDFHS44GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DRUL7T68: SDFHS43GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DRUL15T3: SDFHS41GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6DRUL30T7: SDFHS40GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6DVULxxxx Series: 3 DWPD

KCM6DVUL800G: SDFHQ46GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DVUL1T60: SDFHQ45GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DVUL3T20: SDFHQ44GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DVUL6T40: SDFHQ43GEBxxx

Item	Current	Revised
EC Rev.	A5	A6
FW Rev.	0107	0108

KCM6DVUL12T8: SDFHQ41GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

For Generic, FIPS, KCM6 series

KCM6FRULxxxx Series: 1 DWPD

KCM6FRUL960G: SDFHS66GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FRUL1T92: SDFHS65GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FRUL3T84: SDFHS64GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FRUL7T68: SDFHS63GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FRUL15T3: SDFHS61GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FRUL30T7: SDFHS60GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FVULxxxx Series: 3 DWPD

KCM6FVUL800G: SDFHQ66GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FVUL1T60: SDFHQ65GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FVUL3T20: SDFHQ64GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FVUL6T40: SDFHQ63GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

KCM6FVUL12T8: SDFHQ61GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
FW Rev.	0107	0108

Special Attention for FW-download

To Enable items that described "need power cycle" in "Category" Column, it is necessary power cycle to update 0108 Firmware from 0106 and before as follows.
The first download may take around 6 seconds.
No need power cycle to update 0108 from 0107

Firmware update command sequence to enable some fixes that relate to “need power cycle”.
nvme id-ctrl $DeviceName; check FW revision
nvme fw-download $DeviceName --fw=***(Describe new Firmware name)
nvme fw-commit $DeviceName --action=3
Power cycle.
Wait about 10 seconds.
Power cycle.
Wait about 10 seconds.
nvme id-ctrl $DeviceName; check FW revision

DESCRIPTION OF CHANGE

1. Fixed issues

(1) Write Cache Off

Issue: Timeout occurred during Sanitize in Write Cache Off (WCO) mode.

Cause: Sanitize command is not completed because LUT compaction was disabled in WCO mode.

Fix: If Sanitize command issued during WCO mode, enable LUT compaction and then start processing.

(2) Create/ Delete Namespace

Issue: The drive hangs up by Create/ Delete NS during I/O processing.

Cause: There is a possibility to cause drive hang-up condition due to confliction of I/O and Create NS processing in SoC. Once this hang-up condition observed, the drive cannot respond to any commands, and it might become failure mode since it cannot proceed to PLP process after the power turned off.

Fix: FW is fixed to suspend I/O processing when processing Create/ Delete NS.

(3) Timeout

Issue: PCIe Config Register access could be timeout.

Cause: FW had enabled PCIe interrupts when initializing PCIe module. If PCIe interrupts occur at this time, FW manipulates the module being initialized, leads to be hang-up.

Fix: Fix FW to disable PCIe interrupts while initializing PCIe modules.

(4) SMART

Issue: Get Log Page LID=02h SMART/ Health Information Data Units Read and Host Read Commands are not incremented when executing Fused Compare and Write command.

Cause: Omission in implementation.

Fix: FW fix to add process to update SMART information when Fused Compare and Write command is executed.

(5) PLP

Issue: The drive may get into the failure mode if the Unsafe shutdown was performed during the host Rd/Wr operations.

Cause: In the unsafe shutdown process, PLP operation works and all the necessary system data should be saved to the emergency area. However, certain system data was left over unsaved during the PLP operation, resulting the drive being the failure mode at the drive next power-on.

Fix: Added the appropriate flag to be clearly identified the data to be saved in the PLP operation.

(6) PCIe uncorrectable error

Issue: When the PCIe uncorrectable errors happen, such as UR (Unsupported Request) and/or CA (Completer Abort) from the host, the drive may fail to handle these situations, resulting in the drive hang condition.

Cause: If host responds CA/UR against PRP fetch, drive goes into HW Fatal Error and drive will not be seen anymore. In this case, drive cannot be recovered due to the limitation of architecture.

Fix: When the HW Fatal Error condition happens in the drive side due to the UR/CA response, the new FW performs SoC reset to recover HW Fatal Error condition. This issue exists security drive only (SED/SIE/FIPS).

(7) Timeout

Issue: MCTP command issued after Power Cycle with PERST#Assert-RefClk Off timed out (FW Assert)

Cause: The Abort flag determines whether the response data transfer processing task is enqueued or not at the STOP interrupt after an Abort occurs. Since the response data transfer processing task is enqueued by the Abort interrupt, this flag is used to determine whether or not to enqueue the response data transfer processing task by the STOP interrupt that occurs after the Abort interrupt. The timing for clearing that Abort flag was incorrect.

Fix: Correct the initialization process of the flag to enqueue the transfer processing task so that it is initialized before the start of normal transfer.

(8) Failure mode

Issue: Occasional startup failure occurs after PLP execution.

Cause: When PLP is executed, BE State is not correctly determined, PLP log dump and SA information update check are not performed, and SA information is not updated at PLP, resulting in failure due to information mismatch at the next startup.

Fix: Correct the macro function for BE State determination.

(9) Sanitize

Issue: IO Command cannot respond during Sanitize execution.

Cause: The Drive was trying to transition to Sleep by mistake during Sanitize execution, The drive did not transition to Sleep, but IO execution was prevented.

Fix: Drive does not transition to Sleep by mistake during Sanitize execution.

(10) NVMe-MI

Issue: The response value of Pause Control Primitive to the short MI command response is incorrect.

Cause: The Pause Control Primitive prompts the MI command process to the pause state, but there was no opportunity to move to the pause state during the transmission of the short MI command response (MCTP 1 packet).

Fix: When Pause Control Primitive is processed in a state where it is not possible to pause, the Pause flag is changed so that it is not turned on.

(11) DST

Issue: FW assertion happens at FW Commit during Device Self-Test (DST).

Cause: Power Management IC (PMIC) test of the background DST will create the interrupt to communicate to the CPU. If this interrupt happens during the FW commit process, this interrupt is suspended until the completion of the FW Commitment. After FW Commitment, the new FW detects this suspended interrupt, but the new FW cannot handle this condition, causing the FW assertion.

Fix: FW clears a DST interrupt suspended at the completion of FW Commitment. And, if a communication error happens between SoC and PMIC, then FW aborts PLP capacitor patrol to avoid a command timeout for some commands including FW Commit command.

(12) Timeout

Issue: Write command timeout occurs during HotSwap test.

Cause: HostWrite timed out due to delay in compaction caused by time consuming valid cluster determination during LUT restoration.

Fix: Fix to skip compaction and proceed HostWrite when it takes time to determine valid clusters during LUT restoration.

(13) Uncorrectable Error

Issue: If a power failure occurs during a write operation and a power failure occurs before the drive is ready at subsequent Power ON, the write data may be uncorrected in rare cases when it is read.

Cause: If data is in the process of being written when the power is turned off, the data in the process of being written is stored in the temporally Flash Memory area. And then, when the power is turned on, the data is stored in the proper Flash Memory area. If Power off occurs again during the data store process, however, the data needs to be stored in the temporally Flash Memory area again. In rare cases the wrong data is stored. As a result, when the data is read at the next startup, an uncorrectable error may occur due to data inconsistency.

Fix: Correct the data store process so that wrong data can not be stored when the power is turned off.

(14) SMBUS

Issue: Responding DATA_NACK while issuing Drive Status Data.

Cause: When a STOP reception interrupt of the previous command and a START + Slave Address + R/W bit reception interrupt (AIS) of the next command are received simultaneously, it is correct to process them in the order of STOP of the previous command -> AIS of the next command. However, the order was AIS of the next command, then STOP of the previous command.

Fix: When AIS interrupt and STOP interrupt are notified at the same time, the processing order is changed from AIS -> STOP to STOP -> AIS.

(15) Timeout

Issue: With Power on(boot-up)-RefClk Off, MPR=1 Response of VPD Write command exceeds 100ms.

Cause: When the MCTP command is received, the MPR sending task is started after 80 ms in order to send the MPR reply within 100 ms. However, during the startup process, the task was stuck to the task and there was a period of about 50 ms during which control was not passed to other tasks. 80 ms before the MPR startup, the MPR response timeout occurred.

Fix: During startup, the MPR startup time was changed to 1 ms for immediate response.

(16) Drive boot-up

Issue: Drive may not start if Program fail occurs during GC process at startup. It can recover by Power Cycle.

Cause: The processing step when Program fail occurred in GC during startup was incorrect, and GC processing did not proceed and the system did not become Drive ready.

Fix: Changed the processing step when Program fail occurs in GC during startup.

(17) I2C

Issue: An I2C communication error between SoC and PMIC (Power Management IC) on the drive might occur rarely.

Cause: tHD:DAT (from the falling SCL to the holding SDA) margin in I2C interface was not enough.

Fixed: Changed tHD:DAT margin from 2 nsec to 1 usec to fix this issue.

(18) SMBUS

Issue: While repeatedly executing Get UDID in SMBus, if the Host responds NACK when sending Data from the Drive, the Drive will return NACK for the next Get UDID.

Cause: FW may detect SMBus NACK, STOP, and the next Command reception at the same time, and in this case, FW continues the data transfer to which NACK was returned. In addition, NACK was mistakenly responded to the next Get UDID issued.

Fix: Fix FW to abort the data transfer that returned NACK and execute the next command.

(19) SMBUS

Issue: SDA Low Stuck is not detected and will not accept commands via SMBUS until it is restored by PowerCycle.

Cause: The configuration value for detecting SDA Low Stuck was incorrect. Therefore, even if SDA Stuck at low, Abort does not occur.

Fix: The setting value at register initialization was corrected to detect SDA Low Stuck.

(20) FW download

Issue: If the FW Length in the FW Binary is unexpected value, checking the Binary in the FW Commit command may cause a failure.

Cause: FW's Binary check includes CRC verification, which must be performed in 4Byte width, but FW performs CRC verification even if the value indicating the length of the Binary is not in Byte width. This triggers unauthorized access to the memory, resulting in a state in which PLP processing cannot be performed, leading to fail to failure mode.

Fix: FW fix when verifying FW, add checks for FW length, Data Align of Binary, and Boundary, and report Error if any abnormality is found.

(21) PCIe

Issue: No response from Endpoint Discovery after PCIe conventional reset.

Cause: Discovered Flag is not cleared at PCIe conventional reset.

Fix: When PCIe conventional reset or Link Down occurs, initialize the Endpoint of the concerned port and clear the Discovered Flag.

(22) Uncorrectable Error

Issue: Uncorrectable Read Error occurred during PLP injection test.

Cause: PLP process makes unsaved User Data non-volatile in the temporary area.
When power is turned on, the User Data in the temporary area is rewritten as the original User Data. The possibility of PLP occurring at the time of rewriting was not taken into account, and FTL and User Data could not be correctly linked.
Therefore, when the host received read command after power-on, the data was read from a different location than where the User Data was originally stored, resulting in an Uncorrectable Read Error.

Fix: Fix FW to change the sequence of re-writing User Data in the temporary area as the original User Data.

(23) Sanitize Format NVM

Issue: When the drive is in the Write Protected mode, Sanitize CMD and Format NVM CMD would not operate correctly.

1) When the Sanitize CMD with Block Erase sanitize action is executed, the Sanitize CMD is completed, but the background sanitization will not work correctly.
2) Format CMD sometimes ends with an error.

Cause: The current drive FW is not care about the Write Protected Mode correctly.

Fix:

1) Changed the drive FW to execute background Block Erase operation in the Write Protected mode.
2) Changed the drive FW not to terminate Format CMD when it runs in the Write Protected mode.

(24) SMBUS

Issue: When transferring large data using SMBus with MTU set to a value larger than 248 bytes (249, 250), the command is discarded after the 256th byte has been transferred without completing the transfer.

Cause: When MTU is 249 or 250 bytes, the size of data to be transferred is 257 or 258 bytes including headers and PEC. On the other hand, since only 256 bytes are available in the TX_FIFO, the data that cannot be fully loaded is discarded. As a result, STOP information cannot be sent, and an unexcited timeout interrupt occurs, interrupting the command processing.

Fix: To prevent the size of data to be sent from exceeding the size of TX_FIFO, the maximum value of MTU was changed to 248 bytes, and when switching to a new FW with MTU=249 or 250, the value is updated to MTU=248.

(25) FW download

Issue: When MCTP Reset (OP=07h) command is issued while FW Commit is running (CA=1, Slot=3), while changing the timing of command issuance, the value reported in LogPage (LID=3h) is Slot3, but ActiveSlot does not become Slot3.

Cause: When Reset was executed during FW Commit (CA=1), FW Commit (CA=1) command was Abort and FW Commit (CA=1) command was terminated during FW Commit process.

Fix: FW Commit(CA=1) command Abort confirmation timing has been changed so that it does not Abort after FW Commit(CA=1) FW write process has started.

(26) Drive lost

Issue: The host system may not recognized drives during reboot.

Cause: Internal CPU accessed the same area during another internal CPU initialization processing. it caused an internal inconsistency.

Fix: Prevented another CPU accessing the specific area until the initialization was completed.

(27) PCIe

Issue: The response value of PCIe Command of NVMe-MI is incorrect.

Cause: Issuing "PCIe Configuration Write command (OPCode 01h)" in the PCIe Command category of NVMe-MI results in status=04h (Invalid Parameter). Expected value is status=03h (Invalid Command Opcode) because it is not supported.

Fix: Change to status=03h (Invalid Command Opcode).

(28) CFS

Issue: Reset does not clear CFS.

Cause: Because the CFS register was not cleared on Reset.

Fix: Record which Reset is used to clear CFS when it stands up. When the recorded Reset is executed, CFS is cleared. Changed so that CFS is cleared when a register is cleared in the internal Reset process.

(29) Format NVM

Issue: When the Format NVM command is executed with LBAF=0 and SES=1 for 512 byte/sector without metadata, the drive may report the wrong FLBAS (Formatted LBA size) value 10h in the Identify data structure.

Cause: When the Format NVM command is executed with SES=1 for the User-Data-Erase option, the drive FW mistakenly refers to the MSET (Metadata Settings) in the Format command to build up the FLBAS filed in the Identify dataset.

Fix: Fixed the drive FW to refer to the appropriate field to build the FLBAS in the Identify Namespace dataset.

(30) MCTP

Issue: MCTP command Abort when Controller Reset / FLR occurs.

Cause: The only reset type that does not abort MCTP command was BME Clear.

Fix: Add more reset type which does not abort MCTP command.

(31) Format NVM

Issue: Format command with NSID All Fs handling was not as per NVMe 2.0 specifications.

Cause: NVMe 2.0 Specification changes were not incorporated.

Fix: Format command with NSID all Fs will not fail irrespective of whether namespaces are present or not.

(32) SMART

Issue: The drive reports an error for an unsupported command and increases the Number of Error Entries in SMART/ Health Information when Security CMD is sent by NVMe CLI.

Cause: The current CM6 reports incorrect values in the NIC and NCC bits in the GetLog CMD (LID=0x05). Because of these bits, the NVMe-CLI automatically issues Identify CMD with CNS=06h, which is NOT supported by the CM6, when the customer sends Security CMD by the NVMe-CLI.

Fix: FW is fixed to report NIC=0b/ NCC=0b for Security Send CMD, and NIC=0b/ NCC=0b/ LBCC=0b for Security Receive CMD on the Get Log Page LID=05h (Commands Supported and Effects). LBCC for Security Receive is not directly related to this issue, but has been corrected to the appropriate value.

(33) SMBus

Issue: When the drive is sending the MCTP response over SMBus, if SMBus Serial Data (SDA) stays at low level for a long time, the following MCTP command will end timeout.

Cause: When SDA Low stack is detected by the drive side, the recovery process is started, however the recovery routine does not handle this situation correctly, and cannot recover from the SDA low stack condition.

Fix: Modify the drive FW to be able to handle the SDA low stack condition correctly.

2. Others

(1) SeqR Performance

Change ChopSize from 512k to 2M to improve performance of SeqR TL=2M.

(2) Dataset Management (Standard, SIE only)

Improved the processing time for Dataset Management command to optimize the internal deallocation process.

DATE OF APPLICATION

This change is applied to the factory line from Apr, 2024.

Prepared by:	**M.Ikehata**	M. Ikehata
Checked by:	**S.Rikukawa**	S. R
Approved by:	**T.Masakawa**	Takahiro Masakawa