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EIN No: SSDCM6-037 Rev. A Date: August. 24, 2021 Originator: SSD Design Dept. Group 1

Engineering Information Notice (EIN)

PRODUCT AFFECTED

For Generic, Std/SIE/SED/FIPS KCM6 series

KCM61VULxxxx Series : 3 DWPD
- KCM61VUL800G : SDFHQ06GEAxxx
- KCM61VUL1T60 : SDFHQ05GEAxxx
- KCM61VUL3T20 : SDFHQ04GEAxxx
- KCM61VUL6T40 : SDFHQ03GEAxxx
- KCM61VUL12T8 : SDFHQ01GEAxxx

KCM61RULxxxx Series : 1 DWPD
- KCM61RUL960G : SDFHS06GEAxxx
- KCM61RUL1T92 : SDFHS05GEAxxx
- KCM61RUL3T84 : SDFHS04GEAxxx
- KCM61RUL7T68 : SDFHS03GEAxxx
- KCM61RUL15T3 : SDFHS01GEAxxx
- KCM61RUL30T7 : SDFHS00GEAxxx

KCM6XVULxxxx Series : 3 DWPD
- KCM6XVUL800G : SDFHQ86GEBxxx
- KCM6XVUL1T60 : SDFHQ85GEBxxx
- KCM6XVUL3T20 : SDFHQ84GEBxxx
- KCM6XVUL6T40 : SDFHQ83GEBxxx
- KCM6XVUL12T8 : SDFHQ81GEBxxx

KCM6XRULxxxx Series : 1 DWPD
- KCM6XRUL960G : SDFHS86GEBxxx
- KCM6XRUL1T92 : SDFHS85GEBxxx
- KCM6XRUL3T84 : SDFHS84GEBxxx
- KCM6XRUL7T68 : SDFHS83GEBxxx
- KCM6XRUL15T3 : SDFHS81GEBxxx
- KCM6XRUL30T7 : SDFHS80GEBxxx

KCM6DVULxxxx Series : 3 DWPD
- KCM6DVUL800G : SDFHQ46GEBxxx
- KCM6DVUL1T60 : SDFHQ45GEBxxx
- KCM6DVUL3T20 : SDFHQ44GEBxxx
- KCM6DVUL6T40 : SDFHQ43GEBxxx
- KCM6DVUL12T8 : SDFHQ41GEBxxx

KCM6DRULxxxx Series : 1 DWPD
- KCM6DRUL960G : SDFHS46GEBxxx
- KCM6DRUL1T92 : SDFHS45GEBxxx
- KCM6DRUL3T84 : SDFHS44GEBxxx
- KCM6DRUL7T68 : SDFHS43GEBxxx
- KCM6DRUL15T3 : SDFHS41GEBxxx
- KCM6DRUL30T7 : SDFHS40GEBxxx

KCM6FVULxxxx Series : 3 DWPD
- KCM6FVUL800G : SDFHQ66GEBxxx
- KCM6FVUL1T60 : SDFHQ65GEBxxx
- KCM6FVUL3T20 : SDFHQ64GEBxxx
- KCM6FVUL6T40 : SDFHQ63GEBxxx
- KCM6FVUL12T8 : SDFHQ61GEBxxx

KCM6FRULxxxx Series : 1 DWPD
- KCM6FRUL960G : SDFHS66GEBxxx
- KCM6FRUL1T92 : SDFHS65GEBxxx
- KCM6FRUL3T84 : SDFHS64GEBxxx
- KCM6FRUL7T68 : SDFHS63GEBxxx
- KCM6FRUL15T3 : SDFHS61GEBxxx
- KCM6FRUL30T7 : SDFHS60GEBxxx

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CLASSIFICATION

[☐] Electrical
[☐] Mechanical
[☒] Others

LEVEL

[☐]Hardware
[☒] Software (firmware)
[☐] Document
[☐] Manufacturing
[☐] Others

IMPLEMENTATION

[☒] Factory
[☐] Customer side
[☐] As required
[☐] Repaired
[☐] Retrofit kit required

PRIORITY

[☐] Urgent
[☐] Immediate
[☒] Routine

REVISION LEVEL

■KCM61VULxxxx Series : 3 DWPD

KCM61VUL800G：SDFHQ06GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM61VUL6T40：SDFHQ03GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM61VUL1T60：SDFHQ05GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM61VUL12T8：SDFHQ01GEAxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM61VUL3T20：SDFHQ04GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

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■KCM6XVULxxxx Series : 3 DWPD

KCM6XVUL800G : SDFHQ86GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6XVUL6T40 : SDFHQ83GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6XVUL1T60 : SDFHQ85GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6XVUL12T8 : SDFHQ81GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM6XVUL3T20 : SDFHQ84GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

■KCM6DVULxxxx Series : 3 DWPD

KCM6DVUL800G : SDFHQ46GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6DVUL6T40 : SDFHQ43GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6DVUL1T60 : SDFHQ45GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6DVUL12T8 : SDFHQ41GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM6DVUL3T20 : SDFHQ44GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

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■KCM6FVULxxxx Series : 3 DWPD

KCM6FVUL800G : SDFHQ66GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6FVUL6T40 : SDFHQ63GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6FVUL1T60 : SDFHQ65GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6FVUL12T8 : SDFHQ61GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM6FVUL3T20 : SDFHQ64GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

■KCM61RULxxxx Series : 1 DWPD

KCM61RUL960G : SDFHS06GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM61RUL7T68 : SDFHS03GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM61RUL1T92 : SDFHS05GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM61RUL15T3 : SDFHS01GEAxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM61RUL3T84 : SDFHS04GEAxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM61RUL30T7 : SDFHS00GEAxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK2AA	←
Rev.	B0/C0	←
PCB Code(Daughter)	—	←
Rev.	—	←
FW Rev.	0105	0106

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■KCM6XRULxxxx Series : 1 DWPD

KCM6XRUL960G : SDFHS86GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6XRUL7T68 : SDFHS83GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6XRUL1T92 : SDFHS85GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6XRUL15T3 : SDFHS81GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM6XRUL3T84 : SDFHS84GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6XRUL30T7 : SDFHS80GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK2AA	←
Rev.	B0/C0	←
PCB Code(Daughter)	—	←
Rev.	—	←
FW Rev.	0105	0106

■KCM6DRULxxxx Series : 1 DWPD

KCM6DRUL960G : SDFHS46GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6DRUL7T68 : SDFHS43GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6DRUL1T92 : SDFHS45GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6DRUL15T3 : SDFHS41GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM6DRUL3T84 : SDFHS44GEBxxx

Item	Current	Revised
EC Rev.	A3	A4
PCB Code (Mother)	FKK1VD	←
Rev.	E0/F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6DRUL30T7 : SDFHS40GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK2AA	←
Rev.	B0/C0	←
PCB Code(Daughter)	—	←
Rev.	—	←
FW Rev.	0105	0106

■KCM6FRULxxxx Series : 1 DWPD

KCM6FRUL960G : SDFHS66GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6FRUL7T68 : SDFHS63GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6FRUL1T92 : SDFHS65GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6FRUL15T3 : SDFHS61GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1WD	←
Rev.	F0/G0	←
PCB Code(Daughter)	FKK1ZD	←
Rev.	A0	←
FW Rev.	0105	0106

KCM6FRUL3T84 : SDFHS64GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK1VD	←
Rev.	F0/G0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

KCM6FRUL30T7 : SDFHS60GEBxxx

Item	Current	Revised
EC Rev.	A1	A2
PCB Code (Mother)	FKK2AA	←
Rev.	B0/C0	←
PCB Code(Daughter)	-	←
Rev.	-	←
FW Rev.	0105	0106

Special Attention for FW-download

To Enable items that described "need power cycle" in "Category" Column, it is necessary power cycle to update 0106 Firmware from 0105 as follows.
The first download may take around 6 seconds.

Firmware update command sequence
nvme id-ctrl $DeviceName ; check FW revision
nvme fw-download $DeviceName --fw=***(Describe new Firmware name)
nvme fw-commit $DeviceName --action=3
nvme id-ctrl $DeviceName; check FW revision
Wait about 10 seconds.
Power cycle.

DESCRIPTION OF CHANGE

1. Fixed issues

(1)Command time out
Issue: Write command time out occurred under the combination of Sanitize(Block Erase)/FormatNVM(User Data Erase, Non-SED only), sudden power off, power on and sequential write.
Cause: There was a FW bug, wrong flag setting in the special process of the above combination. Then write command have to wait for a while due to 100% Garbage Collection.
Fix: Fixed the wrong flag setting.

(2)TCG command

Issue: When TCG Command (SecuritySend) is executed under Write Protect Mode, Drive Internal Error occurs.
Cause: The judgment of executing TCG command under Write Protect Mode was incorrect.
Fix: Corrected the judgment.

(3)NVMe-MI

Issue: Drive specification of Read NVMe-MI Data Structure (Optional Commands Supported) does not comply the NVMe specification.
Cause: Wrong report
Response Data Length=2
NUMCMD=00
CMD0 :No report
Fix: Corrected as followings
Response Data Length=4
NUMCMD=00
CMD0=00

(4)Log page

Issue: Drive reports lower data to Log page 09h, Media Units Written than actual data.
Cause: The calculation of Media Units Written for FTL update was incorrect.
Fix: Corrected the calculation of Media Units Written for FTL update.

(5)NVMe-MI

Issue: Response Entries (RENT) of Controller Health Status Poll is 0's based.
Cause: Misunderstood the NVMe specification.
Fix: Fixed to report 1's based

(6)Link up(need power cycle)

Issue: It takes 500ms to become PCIe linkup from Power ON.
Cause: Fixed waiting time, 500ms was set in order to wait for stabilized REFCLK input.
Fix: Link up process starts after detecting REFCLK stabilized.

(7)Time out

Issue: Time out occurs when the host issues the Reset before the drive responses FW commit command completion status.
Cause: There is a case that the drive ignores Reset deassert when Reset is asserted during transferring from old FW to new FW.
Fix: FW does not ignore Reset deassert.

(8)FW download

Issue: There is a case that FW download takes over more than 5 second.
Cause: FW download does not start until the completion of NAND refresh when the drive receives FW download command while NAND refresh is running in background.
Fix: Changed FW to hold background NAND refresh and start FW download immediately once the drive receives FW download command.

(9)Set feature
Issue: When either of Aggregation Time or Aggregation Threshold is 0, Coalescing does not become invalid.
Cause: There was a wrong setting when either of Aggregation Time or Aggregation Threshold is 0.
Fix: Fixed the setting that Coalescing becomes invalid when either of Aggregation Time or Aggregation Threshold is 0.

(10)Set feature
Issue: Aggregation Timer becomes invalid when Aggregation Threshold is set to 0xFF.
Cause: When Aggregation Threshold is set to 0xFF, it's setting is the same as setting 0x00 due to HW bug.
Fix: When Aggregation Threshold is set to 0xFF, FW set it to 0xFE.

(11)Compare/Verify
Issue: 1) The host issues a compare command of PRCHK[0]=1 to Name space formatted by PI Type3, the drive does not response Invalid PI information error.
2) Host issue a verify command of PRCHK[0]=1 to Name space formatted by PI Type1, the drive does not judge as a error even thought there is a deference between 32bits of EILBRT and SLBA.
Cause: 1) When the host issues a compare command of PRCHK[0]=1 to Name space formatted by PI Type3, the drive did not conduct error check.
2) Host issue a verify command of PRCHK[0]=1 to Name space formatted by PI Type1, the drive did not conduct error check.
Fix: 1) The drive to conduct error check.
2)The drive to conduct error check.

(12)Drive hung up
Issue: Drive could be hung up against Reset assert after PCIe Port1 becomes Link disable.
Cause: FW did not clear the error flag when an internal error happens after PCIe Port1 becomes Link disable.
Fix: Revised to clear error flag.

(13)SMBus
Issue: Basic Management Command could be fail due to the load of SMBus.
Cause: Date hold time was no enough during Address phase driven by Host.
Fix: Data latch timing of SDA was shifted by 300ns maximum afterward.

(14)Log page
Issue: When Host designates NUMD=0xffffffff in GetLogPage, the drive reports Invalid Parameter.
Cause: NUMD=0xffffffff makes over flow in the calculation, and the calculation result becomes 0.
Fix: Revised not to become overflow in the calculation.

(15)Admin Command
Issue: Drive could be hang up when the drive received a MI Admin command from SMBus.
Cause: FW assert occurs when receiving a Admin command via SMBus during drive internal resource is not available for Admin command execution. Multiple Admin commands make the drive internal resource exhausted, after that the drive received Admin command from SMBus then, FW assert. occurs.
Fix: FW suspends the MI Admin command execution until the drive internal resource for Admin command execution is available and no FW assert.

(16)Power on process

Issue: When Shut down (CC.SHN=1) and Power on (CC.EN=1) are executed at the timing of NAND error occurring in the NAND refresh process, Power on process may not be completed. After power cycle, the drive can boot up correctly.

Cause: Drive internal condition becomes abnormal, then the drive may hung up when Shut down is requested right after NAND program error occurs in the NAND refresh process.

Fix: Fix the FW to proceed the boot up process correctly.

(17)Persistent event log page"Issue: Header of response data is not returned when Persistent event log page is extracted via MCTP

Cause: The response data is copied to the data sending buffer from the command module that has the response data with a certain offset address. But the calculation of the offset was wrong.

Fix: The offset is calculated correctly.

(18)Set/Get feature

Issue: Drive returns Invalid NS instead of expected Invalid Field in Command when over range NSID is set in Set/Get feature(FID=82h,83h).

Cause: Drive returns wrong information.

Fix: Fix the FW to return Invalid Field in Command when over range NSID is set in Set/Get feature(FID=82h,83h).

(19)Timeout

Issue: PCIe reset process may not proceed and Link down may occur when drive receives PCIe reset while firmware Commit command with commit Action=3h is being executed at FW download.

Cause: When drive receives PCIe Reset after the start of Commit Action process in Firmware Commit command, the Reset process may not receive interruptions due to interruption mask set by the Firmware Commit command. Then Link down may occur.

Fix: Fix the FW to be able to receive interruptions and make PCIe reset process proceed when drive receives PCIe Reset after the start of Commit Action process in Firmware Commit command.

(20)Sanitize

Issue: 1.FW hang-up occurs when Controller Reset is issued during Sanitize operation.

2. Sanitize is aborted when Controller Reset is issued during resumed Sanitize operation.

Cause: 1. When the drive received Controller Reset during a certain period of Sanitize process, the drive releases the allocated Memory in SRAM. However the drive continue to execute Sanitize process and access to released Memory, then hangs up.

2. When Power cycle occurs during Sanitize operation, the Sanitize operation automatically starts from the point it stopped after the power on(resume process). However Controller Reset is issued during the resumed Sanitize process, Sanitize is aborted and is not completed. Then IO hangs up.

Fix: 1.Fix the FW not to check the relevant abort flag not to release the resources.

2. Set a flag in the task at the start of resumed Sanitize operation to prevent the task with the flag from being aborted by Reset.

(21)Response data

Issue: Response data of NVMe-MI Basic Management command is not returned when other than 0x00,0x08,0x20 are specified in Command code.

Cause: FW dose not return response data when other than 0x00,0x08,0x20 are specified in Command code.

Fix: Fix the FW to return response data when 0x00～0xFF are specified in Command code.

(22)Link up

Issue: Link up fail in the special test tool.

Cause: CM6 Link Power Management State entered “Recovery” state from ""L1"" state in 20ms after Device Power Management state became D3hot. Drive ""L1"" state timeout limit was set to 20ms whereas the PCIe specification says it needs 100ms at least.

Fix: ""L1"" state timeout limit was changed to 100ms from 20ms.

(23)Read Data

Issue: Drive may return wrong read data or uncorrectable error after the Host Write command is issued under any one of the following two conditions.

1. 4kB Non-align Unmap (Dataset Management command)
2. L3 correction occurs by 4kB Non-align Read command.

Cause: When write command is issued at any one of above two conditions, a completion of a above condition may change the Host Write control information. As a result, part of LBA of the Host Write command is not written correctly.

Fix: Fix the FW not to change the Host Write control information when the Host Write command and any one of the above two conditions occur at the same time.

(24)Option ROM

Issue: UEFI execution is clashed when Callback is called at UEFI ConfigAccess.

Cause: Callback was not implemented as a member function of ConfigAccess protocol.

Fix: Callback is implemented as a member function of ConfigAccess protocol and drive returns EFI_UNSUPPORTED.

(25)Hang up

Issue: Drive may hung up when multiple errors occur during write operation to Flash Memory by background operation.

Cause: When the background GC (Garbage collection) and background Flash Memory Refresh run, then each has write error at the same time, FW deadlock occurs because error recovery operations conflict with each other.

Fix: Fix the FW not to be deadlock status when the multiple errors occur at the same time.

(26)SMBus

Issue: When drive receives an error interruption from SMBus HW, FW assert may happens and then the drive may hung up. After power cycle, the drive can boot up correctly.

Cause: During drive boot up, the drive accesses to drive internal EEPROM via SMBus.

Although the data transfer to EEPROM is completed, there is a case where the flag that shows data being transmitted continues to be set. When an error interruption from SMBus HW happens rarely, FW recognizes the flag and try to stop the data transfer. However the data transfer is already completed and bring up inconsistency in the FW. Then FW assert occurs.

Fix: FW to clear the flag that shows data being transmitted after completion of accessing to EEPROM in drive boot up process.

2. Added features

(1)Log page

Added the status of Common Clock mode or SRIS, SRNS mode.

Log page Internal Information, F1h offset 100-103

Bytes	Description
103:100	**Refclk Information:**

Bit	Description
32:20	Reserved
19:16	**Clipped maximum link rate:** 0: No limitation 1: Gen1 2: Gen2 3: Gen3 4: Gen4
15:10	Reserved
09	**Force U2:** 0: No limitation 1: Force U.2 mode (U.3 prohibited)
08	**Force common:** 0: No limitation 1: Force common clock mode (SRIS prohibited)
07:03	Reserved
02	**SRIS:** Indicates SRIS mode or not 1: Self-Clock with SSC
01	**SRNS:** Indicates SRNS mode or not 1: Self-Clock and NO SSC
00	**Common Refclk:** Indicates Common Refclk mode or not 1: Common Refclk

3. Others

(1)Option ROM

Drive capacity UNIT is changed from GB to TB at 800GB and 960GB drives on the BIOS display when Option ROM is used.

Max link speed is changed from the current link speed to Gen.4 on the BIOS display.

(2)FIPS

Change COMPLIANCE DESCRIPTOR MODULE NAME(Module name as NIST Web site) from "TC58NC1132GTC" to "KIOXIA TCG OPAL SSC Crypto Sub-Chip TC58NC1132GTC".

(3)VDM

When the drive receives VDM under no Config Wr0, the drive discard the message.

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DATE OF APPLICATION

These changes are applied to the factory line from End of November, 2021

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