ReleaseOrder ID:	*SCGCQ01436900*
Headline:	*Point Release: SAS3FW_Phase15.0 - 15.00.02.00 Fir*
Release Version:	*15.00.02.00*
UCM Project:	*SAS3FW_MASTER_DEV*
Sub UCM Project:	*SAS3FW_Phase15.0*
UCM Stream:	*SAS3FW_Phase15.0_Rel*
Release Type:	*Point*
State:	*Deployed*
Release Baseline:	*SAS3FW_Phase15.0-2017-08-29-15.00.02.00_REL_1504005875@ \SAS_CTRL_FW*
Release Date:	*30-AUG-17*
Date Generated:	*Sep 19, 2017*

Defects Fixed (2):

ID:	SCGCQ01399780
Headline:	With write cache enabled Raid0 volume, SYNC_CHACHE not sent during shutdown.
Description Of Change:	Controller Firmware change the response header based on parameter(Allocation Length) in request. Response Header should be consistent.
Issue Description:	During Shutdown, driver issues SYNC_CACHE allowing the Controller Firmware to pass that command to drives part of write cache enabled volume. This allows drives to flush cache and eliminates data inconsistency after reboot. With the latest Linux Kernel version we are not seeing this SYNC_CACHE, response header sent by Firmware for MODE_SENSE command is not consistent.
Steps To Reproduce:	OS: RedHat 7.2 x64bit. Kernel: 3.10.0-327.e17. x86_64 CPU: Intel(R) Xeon(R) CPU E5-2609 v3 @ 1.90GHz, qty.2 or equivalent HBA card: LSI 3008-IR(FW: P13) Drive: Western Digital Cobra-F (FW: AD02) I confirmed that the WD drive has a large cache of 128 MB. Process: Configure 2 HDDs as RAID0 volume, installation OS and perform cold boot testing.

ID:	SCGCQ01389164 (Port Of Defect SCGCQ01385782)
Headline:	MCTP I2C: I2C communication is lost between BMC and controller
Description Of Change:	Added firmware code to enable and handle the Master Address NAK, Data NAK, and Slave IBML timeout interrupts. Added firmware code to disable the slave receiving when about to transmit I2C Writes. And re-enable slave receiving when a transfer is done. Changed the code to align the addresses of the data buffers used to transmit data. Added stronger synchronization barriers before starting the transfer hardware. Added detection for a certain BMC use-case where it is advantageous for the firmware to automatically Abort an existing command when a new command of the same Application Message Tag comes in.
Issue Description:	The I2C communication is lost between the BMC and controller due to: 1. The transfer hardware with the I2C being used does not recognize some errors, and firmware does not handle either. Includes Master Address NAK, Data NAK, and broken I2C writes to the Slave. 2. FW not managing the transfer hardware using with the I2C in a highly serialized fashion, and with strong enough barriers before starting the transfer
Steps To Reproduce:	With the firmware configured for true MCTP I2C (acts as Master and Slave on the bus) run many request over the bus. Break the bus in various ways to cause the above issues.

Enhancements Implemented (1):

ID:	SCGCQ01423219 (Port Of EnhancementRequest SCGCQ01233843)
Headline:	PL: Implement support for SAS Device Discovery Error Event
Description Of Change:	The firmware will now send SAS Device Discovery Error Events when they are appropriate.