Release Notes: GCA Release: SAS3FW_Phase15.0 - 15.00.00.00 Firmw

ReleaseOrder ID:	***SCGCQ01334300***
Headline:	***GCA Release: SAS3FW_Phase15.0 - 15.00.00.00 Firmw***
Release Version:	***15.00.00.00***
UCM Project:	***SAS3FW_MASTER_DEV***
Sub UCM Project:	***SAS3FW_Phase15.0***
UCM Stream:	***SAS3FW_Phase15.0_Rel***
Release Type:	***GCA***
State:	***Deployed***
Release Baseline:	***SAS3FW_Phase15.0-2017-04-28-15.00.00.00_REL_1493373207@ \SAS_CTRL_FW***
Release Date:	***03-MAY-17***
Date Generated:	***Jul 17, 2017***

Defects Fixed (2):

ID: SCGCQ01323680
Headline: Chassis slot valid bit is not set into Enclosure Page 0.
Description Of Change: 1. Fetched Enclosure handle corresponding to the Device Handle.
2. Stored Chassis details based on Enclosure Handle.
Issue Description: Host requests for Enclosure Page 0 read based on Enclosure Handle, but the firmware has interpreted as Device Handle .
Due to this reason FW has fetched wrong chassis info and updated into Enclosure Page 0.
Steps To Reproduce: 1. Attach a customer specific enclosure to the controller.
2. Read enclosure page 0 for the enclosure attached in 1.
3. Observe that the chassis slot valid bit is not set in the flags field of enclosure page 0.

ID: SCGCQ01334109 (Port Of Defect SCGCQ01316544)
Headline: Cutlass card is not detecting in SLOOB
Description Of Change: ER(SCGCQ01244472) is done to handle the delay during firmware upload as it was calculating the image size for every block request from applications(storelib/sasflash).
As this ER is forcing all applications to calculate image size we are reverting back this ER and making changes in firmware to calculate the image size only once and cache it.
Instead of calculating the image size for every block request, we now calculate the image size only once for first block request and reuse it for all subsequent block requests.
Issue Description: As part of ER(SCGCQ01244472), firmware instead of returning the actual image size now returns region length of flash when it receives FW_UPLOAD request from applications.
Storelib/Sasflash still treat this region length as image size , with no BIOS firmware now returns region size instead of image size as 0.
since applications are not handling the image size, they are not able to list controller information.
Steps To Reproduce: 1. Launch ./storelibtest 73 5
2. Observe cutlass card is not detected in SLOOB.

Note:
1. I2cBusscan is showing the card
2. With PH14 firmware SLOOB detects the card.
3. Attaching sloob logs.

Release History

- **SCGCQ01331893 - GCA Release: SAS3FW_Phase15.0 - 15.00.00.00 Firmw**
- **SCGCQ01321563 - Beta Release: SAS3FW_MASTER_DEV - 14.250.03.00 Fi**
- **SCGCQ01321561 - Beta Release: SAS3FW_MASTER_DEV - 14.250.03.00 Fi**
- **SCGCQ01307674 - Alpha Release: SAS3FW_MASTER_DEV - 14.250.02.00 F**
- **SCGCQ01307672 - Alpha Release: SAS3FW_MASTER_DEV - 14.250.02.00 F**
- **SCGCQ01281044 - Pre-Alpha Release: SAS3FW_MASTER_DEV - 14.250.01.**
- **SCGCQ01281042 - Pre-Alpha Release: SAS3FW_MASTER_DEV - 14.250.01.**

ReleaseOrder ID:	***SCGCQ01331893*** Open In CQWeb
Headline:	***GCA Release: SAS3FW_Phase15.0 - 15.00.00.00 Firmw***
Release Version:	***15.00.00.00***
UCM Project:	***SAS3FW_MASTER_DEV***
Sub UCM Project:	***SAS3FW_Phase15.0***
UCM Stream:	***SAS3FW_Phase15.0_Rel***
Release Type:	***GCA***
State:	***InTest***
Release Baseline:	***SAS3FW_Phase15.0-2017-04-28-15.00.00.00_REL_1493373080@ \SAS_CTRL_FW***
Release Date:	***08-MAY-17***
Date Generated:	***Jul 17, 2017***

Defects Fixed (2):

ID: SCGCQ01323680
Headline: Chassis slot valid bit is not set into Enclosure Page 0.
Description Of Change: 1. Fetched Enclosure handle corresponding to the Device Handle.
2. Stored Chassis details based on Enclosure Handle.
Issue Description: Host requests for Enclosure Page 0 read based on Enclosure Handle, but the firmware has interpreted as Device Handle .
Due to this reason FW has fetched wrong chassis info and updated into Enclosure Page 0.
Steps To Reproduce: 1. Attach a customer specific enclosure to the controller.
2. Read enclosure page 0 for the enclosure attached in 1.
3. Observe that the chassis slot valid bit is not set in the flags field of enclosure page 0.

ID: SCGCQ01334109 (Port Of Defect SCGCQ01316544)
Headline: Cutlass card is not detecting in SLOOB
Description Of Change: ER(SCGCQ01244472) is done to handle the delay during firmware upload as it was calculating the image size for every block request from applications(storelib/sasflash).
As this ER is forcing all applications to calculate image size we are reverting back this ER and making changes in firmware to calculate the image size only once and cache it.
Instead of calculating the image size for every block request, we now calculate the image size only once for first block request and reuse it for all subsequent block requests.
Issue Description: As part of ER(SCGCQ01244472), firmware instead of returning the actual image size now returns region length of flash when it receives FW_UPLOAD request from applications.
Storelib/Sasflash still treat this region length as image size , with no BIOS firmware now returns region size instead of image size as 0.
since applications are not handling the image size, they are not able to list controller information.
Steps To Reproduce: 1. Launch ./storelibtest 73 5
2. Observe cutlass card is not detected in SLOOB.

Note:
1. I2cBusscan is showing the card
2. With PH14 firmware SLOOB detects the card.
3. Attaching sloob logs.

ReleaseOrder ID: ***SCGCQ01321563*** Open In CQWeb
Headline: ***Beta Release: SAS3FW_MASTER_DEV - 14.250.03.00 Fi***
Release Version: ***14.250.03.00***
UCM Project: ***SAS3FW_MASTER_DEV***
Sub UCM Project: ***SAS3FW_Phase15.0***
UCM Stream: ***SAS3FW_MASTER_Invdr_Rel***
Release Type: ***Beta***
State: ***Superseded***
Release Baseline: ***SAS3FW_MASTER_DEV-2017-04-13-14.250.03.00_REL_1492082134@ \SAS_CTRL_FW***
Release Date: ***19-APR-17***
Date Generated: ***Jul 17, 2017***

Defects Fixed (1):

ID: SCGCQ01310561 (Port Of Defect SCGCQ01085128)
Headline: IO Timeout when running IOs and TMs
Description Of Change: When an internal TM completes and there are no resources available to send the completion event to the driver, code was added to send the event when resources become available.
Issue Description: After running a workload of IOs and random TMs, all IO to one device will stop for more than 30 seconds, causing the test to fail.
Steps To Reproduce: Run IOs to a topology with large queue depths and large IO sizes while issuing random TMs to devices such that the controller runs out of resources.

ReleaseOrder ID: ***SCGCQ01321561*** Open In CQWeb
Headline: ***Beta Release: SAS3FW_MASTER_DEV - 14.250.03.00 Fi***
Release Version: ***14.250.03.00***
UCM Project: ***SAS3FW_MASTER_DEV***
Sub UCM Project: ***SAS3FW_Phase15.0***
UCM Stream: ***SAS3FW_MASTER_Invdr_Rel***
Release Type: ***Beta***
State: ***Superseded***
Release Baseline: ***SAS3FW_MASTER_DEV-2017-04-13-14.250.03.00_REL_1492081852@ \SAS_CTRL_FW***
Release Date: ***20-APR-17***
Date Generated: ***Jul 17, 2017***

Defects Fixed (1):

ID: SCGCQ01310561 (Port Of Defect SCGCQ01085128)
Headline: IO Timeout when running IOs and TMs
Description Of Change: When an internal TM completes and there are no resources available to send the completion event to the driver, code was added to send the event when resources become available.
Issue Description: After running a workload of IOs and random TMs, all IO to one device will stop for more than 30 seconds, causing the test to fail.
Steps To Reproduce: Run IOs to a topology with large queue depths and large IO sizes while issuing random TMs to devices such that the controller runs out of resources.

ReleaseOrder ID: ***SCGCQ01307674*** Open In CQWeb
Headline: ***Alpha Release: SAS3FW_MASTER_DEV - 14.250.02.00 F***
Release Version: ***14.250.02.00***
UCM Project: ***SAS3FW_MASTER_DEV***
Sub UCM Project: ***SAS3FW_Phase15.0***
UCM Stream: ***SAS3FW_MASTER_Invdr_Rel***
Release Type: ***Alpha***
State: ***Superseded***
Release Baseline: ***SAS3FW_MASTER_DEV-2017-03-24-14.250.02.00_REL_1490375470@ \SAS_CTRL_FW***
Release Date: ***04-APR-17***
Date Generated: ***Jul 17, 2017***

Defects Fixed (7):

ID: SCGCQ01286998
Headline: Incorrect Copyright Information in NVDATA files
Description Of Change: Copyright information changed from 2016 to 2017 in NVDATA files
Issue Description: Copyright information has to be modified from 2016 to 2017 for Nvdata files
Steps To Reproduce: NA

ID: SCGCQ01294243
Headline: Fix Invader_Main compilation issue after recent update of MPI 2.0.48 headers.
Description Of Change: Removed the reference to the field reserved5 in the code.
Issue Description: After updating the MPI headers to new MPI baseline, found a compilation issue on Invader_Main for accessing reserved5 field of MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0 structure. In latest MPI release, this reserved field has been replaced with new field. Hence we see a compilation issue on Invader_Main.
Steps To Reproduce: N/A

ID: SCGCQ01301927
Headline: IOP: MCTP: Cannot boot and discover controller with PCIe VDM
Description Of Change: Modified the error path to free PCIe credits with MCTP over PCIe VDM enabled.
No longer allowing MCTP Control requests to be processed when the Bus Master Enable is not set with MCTP over PCIe VDM.
Now when the EID in Manufacturing Page 19 is set to NULL, the Get EID indicates only dynamic EID assignment is supported.
Issue Description: Some BIOS in the server family take a long time to enable enable the Bus Master Enable in the PCIe Config Space, which caused a couple of issues.
The server was unable to boot when MCTP over PCIe VDM was enabled. The long delay in the Bus Master enable prevented firmware from responding to MCTP requests over PCIe VDM. An error was hit while processing these requests that caused the credits to not be freed.
Additionally in this situation the bus owner would send a lot of requests that the controller could not legally respond to, but was allowed to process. This de-synchronized the MCTP discovery process as the firmware thought it was discovered and the bus owner had not.
This bus owner also took a strict interpretation of the Get EID command's static EID supported with an EID of NULL, and would cause another discovery de-synchronization.
Steps To Reproduce: Enable MCTP over PCIe VDM on an IT firmware card through NVDATA. Shutdown the server. The server fails to boot, and discover the controller's MCTP capabilities.

ID: SCGCQ01221732 (Port Of Defect SCGCQ01197319)
Headline: Cutlass(16e and 24i) boards are not getting detected on certain non-X86 systems
Description Of Change: Added a NULL check for the Manufacturing Page pointer in the PCIe Interrupt handler path.
Issue Description: There was a recent check added for a Manufacturing Page pointer in the PCIe Interrupt handler path, but this was getting called for a config trap even before the IOC was initialized where the page pointer is NULL. This was causing the controller fault.

Steps To Reproduce: 1. Flash the Cutlass 16i board with the latest Ph14 firmware
2. Connect the board to a non-X86 machine and power on the server.
When machine is powered on, an amber LED glows on the board and controller doesn't get detected under operating system.

ID: SCGCQ01299221 (Port Of Defect SCGCQ01291784)

Headline: PL : Enclosure LEDs won't blink if slot numbers are not sequential

Description Of Change: The slot boundary check which checks if the slot number is greater than the number of array device element is not done if Device Slot number is used.

Issue Description: When the firmware uses 'Device Slot Number'(DSN) for slot Number displaying and slot numbers are not sequential, then the slot boundary check which checks if the slot number is greater than the number of array device elements fails and the request is not processed further. Because of this LEDs wont blink.
The slot boundary check should not be done in case if Device slot number is used.

Steps To Reproduce: ManPage11 AddlFlags is modified to use 'Device Slot Number' for slot Number displaying.

In the enclosure the slot numbers are not sequential.The mapping is having slot numbers from 0-25 and 30-31, slot# 26, 27, 28, 29 are missing.

With the above slot numbering and NVData changes, locate-LED for slot# 30 and 31 won't blink.

ID: SCGCQ01299224 (Port Of Defect SCGCQ01275770)

Headline: PL: BIOS Stuck when firmware is using 'Device Slot Number' for Bay number displaying

Description Of Change: When Firmware adds a request to the Enclosure management queue and the request is failed, message is removed from queue before returning failure.

Issue Description: BIOS is stuck waiting for response from firmware for Enclosure management request.
Firmware adds a request to the Enclosure management queue and does not remove it in cases where firmware fails the request.
In this case, a request is failed as the slot number is not as expected and the message is not removed from the queue.
When another request is received from the BIOS,Firmware queues it behind the message which was not removed but already replied.
This request never gets serviced and gets stuck forever.

Steps To Reproduce: 1. SAS3008 IR controller (9310-8i) is connected to Cobra-R with 4 SAS drives.
2. In the NVData xml file, add ManPage11, AddlFlags = 8 to enable usage of device slot number
3. Use sas2parser to generate binary file for the controller.
4. In the Cobra-R Mfg-XML, update the page "Connector Info Configuration Page" 0xFF05 to start the ConnectorIndex from 0x33 instead of 0x00.
5. During bootup, enter SAS3008 BIOS, and when selecting 'SAS Topology', the BIOS will be stuck.

ID: SCGCQ01304389 (Port Of Defect SCGCQ01264714)

Headline: IOP: Faulting for L2 Cache Correctable Errors

Description Of Change: Changed code to correct the parameter list ordering of the function call, thus ensuring the interrupt was successfully cleared. Additionally, the requirement of implementing a counter was removed as it was determined correctable errors in the L2 Cache is not required to be monitored or fault the firmware.

Issue Description: The controller was encountering an L2 Cache Correctable Error and faulting with a 0x26B6. A counter was previously put in place to only fault when the total number of correctable errors reached 100. However, due to an error in the ordering of the parameter list of a function call, the interrupt was never cleared resulting in the same interrupt counting immediately to 100 and faulting.

Steps To Reproduce: Generate a L2 Cache Correctable Error. The controller faults on the first correctable error encountered.

Enhancements Implemented (35):

ID: SCGCQ00345273

Headline: MPI 2.6: Enclosure Management

Description Of Change: Extended enclosure support to include NVMe.

ID: SCGCQ00853162

Headline: MPI 2.5: Update Description of BiosOptions field in BIOS CONFIG PAGE 1

Description Of Change: Added the following NVDATA bit in order for BIOS to toggle the feature to pull ALT boot device to INT13 Boot List :

MPI2_BIOSPAGE1_OPTIONS_BOOT_LIST_ ADD_ALT_BOOT_DEVICE - Bit 15 in UINT32 BiosOptions field of BIOS Config Page 1 (MPI2_CONFIG_PAGE_BIOS_1)

ID: SCGCQ00915256

Headline: MPI 2.6: Update Ventura family device ids to match latest EDS

Description Of Change: Change 0xAC (Crusader) and 0xAF (Tomcat) defines to match EDS.

ID: SCGCQ00915336

Headline: MPI 2.6: update Marlin-class device IDs

Description Of Change: Added device id defines for Marlin products.

ID: SCGCQ00922213

Headline: MPI 2.6: PCIe IO Unit Page 0 and 1 tweaks

Description Of Change: Updated MPI 2.6 text and added define for MAX_RATE shift.

ID: SCGCQ00925839

Headline: MPI 2.6: Remove all SOP references

Description Of Change: Removed all defines and structure fields related to SOP support.

ID: SCGCQ00948258

Headline: MPI 2.6: Remove all AHCI references

Description Of Change: Removed all defines and structure fields related to AHCI support.

ID: SCGCQ00948955

Headline: MPI 2.6: Add support for SAS-4 and PCIe-4

Description Of Change: Added defines for SAS 4 and PCIe 4 speeds.

ID: SCGCQ00949638

Headline: MPI 2.6: Add Enclosure Level and Connector name to PCIe device page 0

Description Of Change: Added EclosureLevel and ConnectorName fields to PCIe Device Page 0 with the same meaning as SAS Device Page 0.

ID: SCGCQ00954619

Headline: MPI 2.6: add LinkNum field to the PCIe Link configuration pages

Description Of Change: Modified PCIe Link config pages to include a link field.

ID: SCGCQ01009104

Headline: MPI-2.6: backend PCIe feature initialization status reporting

Description Of Change: Added IOCException bit 10 to indicate that backend PCIe device support has been disabled due to an initialization failure and added InitStatus field to PCIe IO Unit Page 1 t provide more detail.

ID: SCGCQ01013930
Headline: MPI 2.6: add flag to force completion queue entry return for NVMe Encapsulated request
Description Of Change: Added Force Admin Error Response (bit

ID: SCGCQ01015826
Headline: MPI2.6: Fix defines that are not unique within the first 32 characters
Description Of Change: Changed defines to be unique within first 32 characters.

ID: SCGCQ01017027
Headline: MPI 2.6: direct reporting of negotiated PCIe link width and speed
Description Of Change: Add Negotiated Link Rate and Negotiated Port Width to PCIe Device page 0.

ID: SCGCQ01018687
Headline: MPI 2.6: Backend SRIS mode enable flag
Description Of Change: Added bit to LinkFlag field of PCIe IO Unit Page 1 PhyData to specify SRIS mode.

ID: SCGCQ01020473
Headline: MPI2.6: Reserve ExtPageTypes for Dragon
Description Of Change: Added comment to header file to indicate reserved ranges.

ID: SCGCQ01063009
Headline: MPI2.6: Add x16 PCI support for Marlin family products
Description Of Change: Added x16 PCI support for Marlin family products by adding x16 width to IO Unit Page 7.

ID: SCGCQ01071374
Headline: MPI2.6: Fix PCI device page enclosure level/connector name to match SAS device page
Description Of Change: Modified PCIe Device Page 0 declaration to match SAS Device Page 0.

ID: SCGCQ01085073
Headline: MPI 2.5: Add new connector types
Description Of Change: Updated MPI2.5 and MPI2.6 specifications and headers with new connector types.

ID: SCGCQ01092340
Headline: MPI 2.6: Modify "SAS IO Unit Page 11" to add a new field "SATAHintingTimeout"
Description Of Change: Updated header file to include SATADeviceWait time to IO Unit page 11.

ID: SCGCQ01116837
Headline: MPI 2.6: Add Sea Arch class and Product IDs
Description Of Change: Added defines to MPI 2.6 specification for the 4008 product and Sea architecture class.

ID: SCGCQ01136127
Headline: MPI2.6: Added new image type and flash region definitions
Description Of Change: Added new definitions for the ImageType field of FwDownload and FwUpload messages. Also, added new flash region definitions for the Flash Layout Extended Image Data.

ID: SCGCQ01141732
Headline: MPI 2.6: Add new clean tool options
Description Of Change: Added new values for the Flags field of Toolbox Clean Tool Request message.

ID: SCGCQ01146583
Headline: MPI 2.6: Add two new reason codes to Active Cable Exception Event Data
Description Of Change: Added reason codes MPI26_EVENT_ACTIVE_CABLE_PRESENT and MPI26_EVENT_ACTIVE_CABLE_DEGRADED to Active Cable Exception Event Data.

ID: SCGCQ01180886
Headline: MPI 2.5 and 2.6: Need IT FW to send new event for expander failing SMP
Description Of Change: IOC would send an event notifying the host that an expander device either failed or timed out a SMP command issued by the IOC even after maximum retries.

ID: SCGCQ01198341
Headline: PL:Customer specific drive enumeration
Description Of Change: 1. As per the new customer specific chassis,it will have two sled storage installed in it .Each sled plugged into different slot of chassis.
Host application like Preboot, BIOS/UEFI will need the (Chassis-Slot-Number: Device-Slot-Number) for reporting location of a device under the chassis.
Chassis-Slot-Number can be used only when Chassis-Slot valid bit is set.

2. As part of Expander discovery process Chassis-Slot-Number and chassis valid bit will be populated based on Vendor Specific part of
SMP_FUNCTION_REPORT_MANUFACTURER_INFORMATION.

3. If host requests for SAS Enclosure Page 0 to get the Chassis Slot number then FW would update Chassis Slot with additional info Chassis Slot Valid bit .

ID: SCGCQ01208954
Headline: MPI 2.5: Add two new reason codes to Active Cable Exception Event Data
Description Of Change: Added Active Cable Exception Event to MPI2.5 specification. Updated header files to provide MPI2.5 definitions.

ID: SCGCQ01213028
Headline: MPI 2.5 : Add support for reporting Chassis Slot to Enclosure Page 0
Description Of Change: Updated MPI2.5 specification to report ChassisSlot in SAS Enclosure Page 0. Update header files for the same.

ID: SCGCQ01213267
Headline: MPI2.6: Mfg7 support for arbitrary starting slot number
Description Of Change: Updated MPI2.6 specification for Manufacturing Page 7 to allow for arbitrary starting slot number. Also, added MPI2_MANPAGE7_SLOT_UNKNOWN definition to the header file.

ID: SCGCQ01223505

Headline: IOP: MCTP: Add NVDATA bit to check for bad packet settings in MCTP Control packet, and send error

Description Of Change: Added a new NVDATA bit to Manufacturing Page 19 (Flags field bit 10). Setting this bit allows firmware to send an MCTP Control response with Completion Code set to Error when a bad Start of Message and End of Message combination occurs in a received MCTP Control request.
This new configurable response behavior enables MCTP Bus Masters to know when a malformed request was sent to the controller firmware by providing error feedback through the standard MCTP Control responses.

Clearing this new bit causes firmware to drop the packet silently.

ID: SCGCQ01223839

Headline: IOP: MCTP: Add NVDATA timeout parameter on message re-assembly

Description Of Change: Added a new MsgAssemblyTimeout field to Manufacturing Page 19. This specifies the number of seconds for the message assembly/re-assembly to time out after the last received packet. If no other packets are sent and the End Of Message packet was not sent, then the message assembly is timed out.

At that point, firmware is free to abort that message and reuse the resources for different message.

ID: SCGCQ01223844

Headline: IOP: MCTP: Add configuration item to have Aborts generate responses

Description Of Change: Added new capability and capability configuration commands, and NVDATA (Manufacturing Page 19) to allow Abort PayloadIDs to generate responses upon completion.

If enabled either through Manufacturing Page 19 or a capability configuration command:
1. A successful Abort will simply return another Abort with that Tag Owner bit cleared.
2. A failed Abort due to a command without the AppMsgTag will return a Packet Exception AppMsgTag Does Not Exist.

The new capability related commands are:
1. Get Capability: Obtains information about a specified SCS MCTP capability.
2. Get Capability Configuration: Obtains the current configuration of a specified SCS MCTP capability.
3. Set Capability Configuration: Modifies the current configuration of a specified SCS MCTP capability.

SCS MCTP capabilities include:
1. VDM Buffer: The VDM Buffer feature implemented by the Set VDM Buffer and Get VDM Buffer commands.
2. Abort: The Abort capabilities, which include the Abort response generation feature

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ID: SCGCQ01258005

Headline: MPI 2.6: Add new firmware download type (CBB BACKUP)

Description Of Change: Updated MPI2.6 specification to add Common Boot Block Image Backup to the ImageType field of FwDownload Request Message. Added MPI2_FW_DOWNLOAD_ITYPE_CBB_BACKUP to the header file.

ID: SCGCQ01304887

Headline: Disable PUIS(Power up in standby) feature support

Description Of Change: PUIS feature support has been disabled.

ID: SCGCQ01282352 (Port Of EnhancementRequest SCGCQ01214813)

Headline: PL: Addition of Cable Exception events

Description Of Change: Added PL interface for sending cable exception events.

Added 2 new Cable Exception events,
1. Cable Present
2. Cable Degraded

ReleaseOrder ID: ***SCGCQ01307672*** Open In CQWeb

Headline: ***Alpha Release: SAS3FW_MASTER_DEV - 14.250.02.00 F***

Release Version: ***14.250.02.00***

UCM Project: ***SAS3FW_MASTER_DEV***

Sub UCM Project: ***SAS3FW_Phase15.0***

UCM Stream: ***SAS3FW_MASTER_Invdr_Rel***

Release Type: ***Alpha***

State: ***Superseded***

Release Baseline: ***SAS3FW_MASTER_DEV-2017-03-24-14.250.02.00_REL_1490375264@\SAS_CTRL_FW***

Release Date: ***30-MAR-17***

Date Generated: ***Jul 17, 2017***

Defects Fixed (7):

ID: SCGCQ01286998

Headline: Incorrect Copyright Information in NVDATA files

Description Of Change: Copyright information changed from 2016 to 2017 in NVDATA files

Issue Description: Copyright information has to be modified from 2016 to 2017 for Nvdata files

Steps To Reproduce: NA

ID: SCGCQ01294243

Headline: Fix Invader_Main compilation issue after recent update of MPI 2.0.48 headers.

Description Of Change: Removed the reference to the field reserved5 in the code.

Issue Description: After updating the MPI headers to new MPI baseline, found a compilation issue on Invader_Main for accessing reserved5 field of MPI2_CONFIG_PAGE_SAS_ENCLOSURE_0 structure. In latest MPI release, this reserved field has been replaced with new field. Hence we see a compilation issue on Invader_Main.

Steps To Reproduce: N/A

ID: SCGCQ01301927

Headline: IOP: MCTP: Cannot boot and discover controller with PCIe VDM

Description Of Change: Modified the error path to free PCIe credits with MCTP over PCIe VDM enabled.
No longer allowing MCTP Control requests to be processed when the Bus Master Enable is not set with MCTP over PCIe VDM.
Now when the EID in Manufacturing Page 19 is set to NULL, the Get EID indicates only dynamic EID assignment is supported.

Issue Description: Some BIOS in the server family take a long time to enable enable the Bus Master Enable in the PCIe Config Space, which caused a couple of issues.
The server was unable to boot when MCTP over PCIe VDM was enabled. The long delay in the Bus Master enable prevented firmware from responding to MCTP requests over PCIe VDM. An error was hit while processing these requests that caused the credits to not be freed.
Additionally in this situation the bus owner would send a lot of requests that the controller could not legally respond to, but was allowed to process. This de-synchronized the MCTP discovery process as the firmware thought it was discovered and the bus owner had not.
This bus owner also took a strict interpretation of the Get EID command's static EID supported with an EID of NULL, and would cause another discovery de-synchronization.

Steps To Reproduce: Enable MCTP over PCIe VDM on an IT firmware card through NVDATA. Shutdown the server. The server fails to boot, and discover the controller's MCTP capabilities.

ID: SCGCQ01221732 (Port Of Defect SCGCQ01197319)

Headline: Cutlass(16e and 24i) boards are not getting detected on certain non-X86 systems

Description Of Change: Added a NULL check for the Manufacturing Page pointer in the PCIe Interrupt handler path.

Issue Description: There was a recent check added for a Manufacturing Page pointer in the PCIe Interrupt handler path, but this was getting called for a config trap even before the IOC was initialized where the page pointer is NULL. This was causing the controller fault.

Steps To Reproduce: 1. Flash the Cutlass 16i board with the latest Ph14 firmware
2. Connect the board to a non-X86 machine and power on the server.
When machine is powered on, an amber LED glows on the board and controller doesn't get detected under operating system.

ID: SCGCQ01299221 (Port Of Defect SCGCQ01291784)

Headline: PL : Enclosure LEDs won't blink if slot numbers are not sequential

Description Of Change: The slot boundary check which checks if the slot number is greater than the number of array device element is not done if Device Slot number is used.

Issue Description: When the firmware uses 'Device Slot Number'(DSN) for slot Number displaying and slot numbers are not sequential, then the slot boundary check which checks if the slot number is greater than the number of array device elements fails and the request is not processed further. Because of this LEDs wont blink.
The slot boundary check should not be done in case if Device slot number is used.

Steps To Reproduce: ManPage11 AddlFlags is modified to use 'Device Slot Number' for slot Number displaying.

In the enclosure the slot numbers are not sequential.The mapping is having slot numbers from 0-25 and 30-31, slot# 26, 27, 28, 29 are missing.

With the above slot numbering and NVData changes, locate-LED for slot# 30 and 31 won't blink.

ID: SCGCQ01299224 (Port Of Defect SCGCQ01275770)

Headline: PL: BIOS Stuck when firmware is using 'Device Slot Number' for Bay number displaying

Description Of Change: When Firmware adds a request to the Enclosure management queue and the request is failed, message is removed from queue before returning failure.

Issue Description: BIOS is stuck waiting for response from firmware for Enclosure management request.
Firmware adds a request to the Enclosure management queue and does not remove it in cases where firmware fails the request.
In this case, a request is failed as the slot number is not as expected and the message is not removed from the queue.
When another request is received from the BIOS,Firmware queues it behind the message which was not removed but already replied.
This request never gets serviced and gets stuck forever.

Steps To Reproduce: 1. SAS3008 IR controller (9310-8i) is connected to Cobra-R with 4 SAS drives.
2. In the NVData xml file, add ManPage11, AddlFlags = 8 to enable usage of device slot number
3. Use sas2parser to generate binary file for the controller.
4. In the Cobra-R Mfg-XML, update the page "Connector Info Configuration Page" 0xFF05 to start the ConnectorIndex from 0x33 instead of 0x00.
5. During bootup, enter SAS3008 BIOS, and when selecting 'SAS Topology', the BIOS will be stuck.

ID: SCGCQ01304389 (Port Of Defect SCGCQ01264714)

Headline: IOP: Faulting for L2 Cache Correctable Errors

Description Of Change: Changed code to correct the parameter list ordering of the function call, thus ensuring the interrupt was successfully cleared. Additionally, the requirement of implementing a counter was removed as it was determined correctable errors in the L2 Cache is not required to be monitored or fault the firmware.

Issue Description: The controller was encountering an L2 Cache Correctable Error and faulting with a 0x26B6. A counter was previously put in place to only fault when the total number of correctable errors reached 100. However, due to an error in the ordering of the parameter list of a function call, the interrupt was never cleared resulting in the same interrupt counting immediately to 100 and faulting.

Steps To Reproduce: Generate a L2 Cache Correctable Error. The controller faults on the first correctable error encountered.

Enhancements Implemented (35):

ID: SCGCQ00345273

Headline: MPI 2.6: Enclosure Management

Description Of Change: Extended enclosure support to include NVMe.

ID: SCGCQ00853162

Headline: MPI 2.5: Update Description of BiosOptions field in BIOS CONFIG PAGE 1

Description Of Change: Added the following NVDATA bit in order for BIOS to toggle the feature to pull ALT boot device to INT13 Boot List :

MPI2_BIOSPAGE1_OPTIONS_BOOT_LIST_ ADD_ALT_BOOT_DEVICE - Bit 15 in UINT32 BiosOptions field of BIOS Config Page 1 (MPI2_CONFIG_PAGE_BIOS_1)

ID: SCGCQ00915256

Headline: MPI 2.6: Update Ventura family device ids to match latest EDS

Description Of Change: Change 0xAC (Crusader) and 0xAF (Tomcat) defines to match EDS.

ID: SCGCQ00915336

Headline: MPI 2.6: update Marlin-class device IDs

Description Of Change: Added device id defines for Marlin products.

ID: SCGCQ00922213

Headline: MPI 2.6: PCIe IO Unit Page 0 and 1 tweaks

Description Of Change: Updated MPI 2.6 text and added define for MAX_RATE shift.

ID: SCGCQ00925839

Headline: MPI 2.6: Remove all SOP references

Description Of Change: Removed all defines and structure fields related to SOP support.

ID: SCGCQ00948258

Headline: MPI 2.6: Remove all AHCI references

Description Of Change: Removed all defines and structure fields related to AHCI support.

ID: SCGCQ00948955

Headline: MPI 2.6: Add support for SAS-4 and PCIe-4

Description Of Change: Added defines for SAS 4 and PCIe 4 speeds.

ID: SCGCQ00949638

Headline: MPI 2.6: Add Enclosure Level and Connector name to PCIe device page 0

Description Of Change: Added EclosureLevel and ConnectorName fields to PCIe Device Page 0 with the same meaning as SAS Device Page 0.

ID: SCGCQ00954619

Headline: MPI 2.6: add LinkNum field to the PCIe Link configuration pages

Description Of Change: Modified PCIe Link config pages to include a link field.

ID: SCGCQ01009104

Headline: MPI-2.6: backend PCIe feature initialization status reporting

Description Of Change: Added IOCException bit 10 to indicate that backend PCIe device support has been disabled due to an initialization failure and added InitStatus field to PCIe IO Unit Page 1 t provide more detail.

ID: SCGCQ01013930
Headline: MPI 2.6: add flag to force completion queue entry return for NVMe Encapsulated request
Description Of Change: Added Force Admin Error Response (bit

ID: SCGCQ01015826
Headline: MPI2.6: Fix defines that are not unique within the first 32 characters
Description Of Change: Changed defines to be unique within first 32 characters.

ID: SCGCQ01017027
Headline: MPI 2.6: direct reporting of negotiated PCIe link width and speed
Description Of Change: Add Negotiated Link Rate and Negotiated Port Width to PCIe Device page 0.

ID: SCGCQ01018687
Headline: MPI 2.6: Backend SRIS mode enable flag
Description Of Change: Added bit to LinkFlag field of PCIe IO Unit Page 1 PhyData to specify SRIS mode.

ID: SCGCQ01020473
Headline: MPI2.6: Reserve ExtPageTypes for Dragon
Description Of Change: Added comment to header file to indicate reserved ranges.

ID: SCGCQ01063009
Headline: MPI2.6: Add x16 PCI support for Marlin family products
Description Of Change: Added x16 PCI support for Marlin family products by adding x16 width to IO Unit Page 7.

ID: SCGCQ01071374
Headline: MPI2.6: Fix PCI device page enclosure level/connector name to match SAS device page
Description Of Change: Modified PCIe Device Page 0 declaration to match SAS Device Page 0.

ID: SCGCQ01085073
Headline: MPI 2.5: Add new connector types
Description Of Change: Updated MPI2.5 and MPI2.6 specifications and headers with new connector types.

ID: SCGCQ01092340
Headline: MPI 2.6: Modify "SAS IO Unit Page 11" to add a new field "SATAHintingTimeout"
Description Of Change: Updated header file to include SATADeviceWait time to IO Unit page 11.

ID: SCGCQ01116837
Headline: MPI 2.6: Add Sea Arch class and Product IDs
Description Of Change: Added defines to MPI 2.6 specification for the 4008 product and Sea architecture class.

ID: SCGCQ01136127
Headline: MPI2.6: Added new image type and flash region definitions
Description Of Change: Added new definitions for the ImageType field of FwDownload and FwUpload messages. Also, added new flash region definitions for the Flash Layout Extended Image Data.

ID: SCGCQ01141732
Headline: MPI 2.6: Add new clean tool options
Description Of Change: Added new values for the Flags field of Toolbox Clean Tool Request message.

ID: SCGCQ01146583
Headline: MPI 2.6: Add two new reason codes to Active Cable Exception Event Data
Description Of Change: Added reason codes MPI26_EVENT_ACTIVE_CABLE_PRESENT and MPI26_EVENT_ACTIVE_CABLE_DEGRADED to Active Cable Exception Event Data.

ID: SCGCQ01180886
Headline: MPI 2.5 and 2.6: Need IT FW to send new event for expander failing SMP
Description Of Change: IOC would send an event notifying the host that an expander device either failed or timed out a SMP command issued by the IOC even after maximum retries.

ID: SCGCQ01198341
Headline: PL:Customer specific drive enumeration
Description Of Change: 1. As per the new customer specific chassis,it will have two sled storage installed in it .Each sled plugged into different slot of chassis.
Host application like Preboot, BIOS/UEFI will need the (Chassis-Slot-Number: Device-Slot-Number) for reporting location of a device under the chassis.
Chassis-Slot-Number can be used only when Chassis-Slot valid bit is set.

2. As part of Expander discovery process Chassis-Slot-Number and chassis valid bit will be populated based on Vendor Specific part of
SMP_FUNCTION_REPORT_MANUFACTURER_INFORMATION.

3. If host requests for SAS Enclosure Page 0 to get the Chassis Slot number then FW would update Chassis Slot with additional info Chassis Slot Valid bit .

ID: SCGCQ01208954
Headline: MPI 2.5: Add two new reason codes to Active Cable Exception Event Data
Description Of Change: Added Active Cable Exception Event to MPI2.5 specification. Updated header files to provide MPI2.5 definitions.

ID: SCGCQ01213028
Headline: MPI 2.5 : Add support for reporting Chassis Slot to Enclosure Page 0
Description Of Change: Updated MPI2.5 specification to report ChassisSlot in SAS Enclosure Page 0. Update header files for the same.

ID: SCGCQ01213267
Headline: MPI2.6: Mfg7 support for arbitrary starting slot number
Description Of Change: Updated MPI2.6 specification for Manufacturing Page 7 to allow for arbitrary starting slot number. Also, added MPI2_MANPAGE7_SLOT_UNKNOWN definition to the header file.

ID: SCGCQ01223505

Headline: IOP: MCTP: Add NVDATA bit to check for bad packet settings in MCTP Control packet, and send error

Description Of Change: Added a new NVDATA bit to Manufacturing Page 19 (Flags field bit 10). Setting this bit allows firmware to send an MCTP Control response with Completion Code set to Error when a bad Start of Message and End of Message combination occurs in a received MCTP Control request.
This new configurable response behavior enables MCTP Bus Masters to know when a malformed request was sent to the controller firmware by providing error feedback through the standard MCTP Control responses.

Clearing this new bit causes firmware to drop the packet silently.

ID: SCGCQ01223839

Headline: IOP: MCTP: Add NVDATA timeout parameter on message re-assembly

Description Of Change: Added a new MsgAssemblyTimeout field to Manufacturing Page 19. This specifies the number of seconds for the message assembly/re-assembly to time out after the last received packet. If no other packets are sent and the End Of Message packet was not sent, then the message assembly is timed out.

At that point, firmware is free to abort that message and reuse the resources for different message.

ID: SCGCQ01223844

Headline: IOP: MCTP: Add configuration item to have Aborts generate responses

Description Of Change: Added new capability and capability configuration commands, and NVDATA (Manufacturing Page 19) to allow Abort PayloadIDs to generate responses upon completion.

If enabled either through Manufacturing Page 19 or a capability configuration command:
1. A successful Abort will simply return another Abort with that Tag Owner bit cleared.
2. A failed Abort due to a command without the AppMsgTag will return a Packet Exception AppMsgTag Does Not Exist.

The new capability related commands are:
1. Get Capability: Obtains information about a specified SCS MCTP capability.
2. Get Capability Configuration: Obtains the current configuration of a specified SCS MCTP capability.
3. Set Capability Configuration: Modifies the current configuration of a specified SCS MCTP capability.

SCS MCTP capabilities include:
1. VDM Buffer: The VDM Buffer feature implemented by the Set VDM Buffer and Get VDM Buffer commands.
2. Abort: The Abort capabilities, which include the Abort response generation feature

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ID: SCGCQ01258005

Headline: MPI 2.6: Add new firmware download type (CBB BACKUP)

Description Of Change: Updated MPI2.6 specification to add Common Boot Block Image Backup to the ImageType field of FwDownload Request Message. Added MPI2_FW_DOWNLOAD_ITYPE_CBB_BACKUP to the header file.

ID: SCGCQ01304887

Headline: Disable PUIS(Power up in standby) feature support

Description Of Change: PUIS feature support has been disabled.

ID: SCGCQ01282352 (Port Of EnhancementRequest SCGCQ01214813)

Headline: PL: Addition of Cable Exception events

Description Of Change: Added PL interface for sending cable exception events.

Added 2 new Cable Exception events,
1. Cable Present
2. Cable Degraded

ReleaseOrder ID: ***SCGCQ01281044*** Open In CQWeb

Headline: ***Pre-Alpha Release: SAS3FW_MASTER_DEV - 14.250.01.***

Release Version: ***14.250.01.00***

UCM Project: ***SAS3FW_MASTER_DEV***

Sub UCM Project: ***SAS3FW_Phase15.0***

UCM Stream: ***SAS3FW_MASTER_Invdr_Rel***

Release Type: ***Pre-Alpha***

State: ***Superseded***

Release Baseline: ***SAS3FW_MASTER_DEV-2017-02-21-14.250.01.00_REL_1487664816@ \SAS_CTRL_FW***

Release Date: ***22-FEB-17***

Date Generated: ***Jul 17, 2017***

Defects Fixed (11):

ID: SCGCQ01201578 (Port Of Defect SCGCQ01189751)

Headline: IOP: MCTP: In I2C slave response mode low level errors can have two responses

Description Of Change: Modified the code in the common path for Packet Exceptions to always check for the default response and remove it if the Packet Exception is not the default response.

Issue Description: When MCTP over I2C is configured exclusively as a slave (slave response mode), low level errors like a Packet Integrity Check or PEC (CRC check) failure can have two responses loaded: the Packet Exception (PE) FW In Wrong State and the one just generated. The default response (PE FW In Wrong State) should have been removed.

Steps To Reproduce: Send FW a request with a bad CRC, or cause the bus to corrupt the packet. Perform two I2C reads. The reader will see the first one will be PE FW In Wrong State and the second as PE PEC Failure.

ID: SCGCQ01201579 (Port Of Defect SCGCQ01196986)

Headline: IOP: MCTP: Heavy traffic from host with operations that take a long time can cause controller to stop acknowledging I2C transactions

Description Of Change: Streamlined the interrupt code and modified to reconfigure the I2C hardware to receive an I2C Write when:
1. The I2C byte buffering is not active
2. A start for an I2C write was received
3. Either the I2C write has been stopped or it was NAKed by the I2C hardware

Issue Description: The issue occurs with MCTP over I2C in slave response mode (always an I2C slave).

When heavy traffic with the operations taking a long time occur from a host, particularly multiple MPI FW Upload commands, the firmware can become out of sync with the I2C interrupt handler. Eventually, this leads to firmware no longer receiving interrupts when the I2C hardware receives a new packet because the packets are not being acknowledged. This results in I2C Writes no longer being acknowledged by the controller.

Steps To Reproduce: Run the MCTP I2C in slave response mode and poll on the controller with some command.
Run "sas3flash -c <X> -list" in a loop (at least 6 times), or some other command on the host to generate MPI FW Upload requests.
The MCTP I2C traffic starts seeing acknowledgement errors and the controller stops responding to I2C transactions.

ID: SCGCQ01204905 (Port Of Defect SCGCQ01155407)

Headline: PL fault 5854 seen when system boots with all SATA drives in setup spun down

Description Of Change: Reverted first command for SATA Initialization that was prior to SMR support, where we sent IDENTIFY as the first command, instead of read Block Device Characteristics log page. Rearranged the SATA Initialization sequence to read the Block Device Characteristics log page after the check power mode to avoid checking any initial command failures during SATA initialization.

Issue Description: As part of SMR drive support we had added a new command to read the Block Device Characteristics log page at the start of the SATA Initialization process, replacing the IDENTIFY as the 1st command. We were also not checking for all the errors and command failures of the block device characteristics log page since this was supposed to fail for NON SMR devices. But we also happened to not check for errors related to command not transferred, timeout, drive errors and etc. This lead to further commands sent to drive, though errors were logged in the hardware leading to faults.

Steps To Reproduce: 1. Large configof SATA HDDs. OS on VD on the controller
2. Mark all the PDs Prepare for Removal except OS VD and make sure they are in spundown mode
3. Reboot the server and see if the OS boot fails

ID: SCGCQ01205282 (Port Of Defect SCGCQ01172334)

Headline: PL SATA Only: outstanding SATA passthorugh IO can cause target reset from timer callback check if sata Initialization not done yet

Description Of Change: In timer call back, do not initiate TM immediately if IO is SATA Pass Through command.
Instead initiate TM if the same Passthrough IO still exists even after 4s. Delay initiating TM to make sure IO is stuck.

Issue Description: A SATA Passthrough command issued to a SATA drive requiring initialization results in the controller resetting the SATA drive and failing the passthrough command

Steps To Reproduce: Only issue SATA passthrough IO to SATA drive without any TUR/Report LUN etc.

ID: SCGCQ01220121 (Port Of Defect SCGCQ01219591)

Headline: IOP: MCTP I2C: FW Download sometimes causes controller to be unresponsive

Description Of Change: Modified the I2C receive packet code so that it properly clears out the I2C hardware when multiple I2C packets were missed by the firmware. This code is used when the firmware is trying to receive a new I2C packet.

Issue Description: When an MPI FW Download request is issued to the firmware to update the controller firmware, the I2C interface for MCTP can sometimes become unresponsive. This is because the firmware was not able to process the packets in the I2C hardware while erasing the flash.

Steps To Reproduce: Send an MPI FW Download request.
Continue I2C MCTP operations at the same time.

ID: SCGCQ01221731 (Port Of Defect SCGCQ01150838)

Headline: IOP: MCTP: application sees unexpected severe errors for removed/not registered drives and reset controller

Description Of Change: Controller firmware now sends an MPI SCSI IO reply with IOC Status SCSI Device Not Registered when a device is no longer registered, but a SCSI IO was sent to the device.

When a fault or reset occurs, then disable the MCTP related hardware. This will cause previous I2C bus errors to become I2C address NAK errors.

Issue Description: An MCTP application is seeing severe errors under one of two conditions:
1. A drive is removed or not registered, but a SCSI IO is sent to the drive from the MCTP application before a remove event occurs
- Firmware sends a Command Status Invalid Parameter
2. The controller is under reset, and an I2C bus error occurs when the MCTP application performs and I2C operation it sees bus errors for a a time

Steps To Reproduce: Configure the controller for MCTP over I2C in slave response mode.

For error #1, remove a drive, and then send a SCSI IO to the removed drive through MCTP over I2C.

For error #2, reset or fault the controller, and then send MCTP over I2C traffic tot he controller.

ID: SCGCQ01226356 (Port Of Defect SCGCQ01218943)

Headline: (SATA Only) PL fault 5854 seen when system boots with specific SATA drives spun down

Description Of Change: Block Device Characteristics log page is not supported by many new model drives but is needed to be called to detect if it's SMR or not. In most cases of SATA drives this command fails or times out, even in the case where drives are spun down. So firmware should not be stopping the SATA Initialization for the response from Block Device Characteristics log page , but allow the next set of commands to be sent and allow those commands to stop the SATA Initialization, if needed.

Issue Description: For Spun down SATA drives initial commands during SATA Initialization are completed and firmware also tries to read Block Device Characteristics log page, which fails or times out and thus the command is failed. Some specific bad drives maybe responding post timeout and causing error as the command and context is already freed.

Steps To Reproduce: 1. Connect large number of SATA drives of specific manufacturer to the controller.
2. Spin down all the SATA drives.
3. Reboot the server or reset the controller and observe Fault 0x5854

ID: SCGCQ01259543 (Port Of Defect SCGCQ01041762)

Headline: PL: SAS 3008 controller crash - fault_state(0x584a)

Description Of Change: Modified firmware so we check for this hang condition. When detected, we clear the areas responsible, target reset the device, and continue.

Issue Description: While running stress to all devices in the topology, there exists a possibility in which the data payload of a data frame may be wiped out, but the CRC is still valid. When this occurs, our controller hangs until a timeout condition occurs resulting in a fault.

Steps To Reproduce: 1. Run IO to all devices in the topology.
2. Using a SAS Jammer, inject the following error into the data stream:
   a. Trigger on an incoming data frame.
   b. Remove the data payload from the frame.
   c. re-calculate the CRC, so it is valid

ID: SCGCQ01263737 (Port Of Defect SCGCQ01253195)

Headline: PL Fault 0x5813 caused during SEND FSM TIMEOUT interrupt handling

Description Of Change: Avoided interrupt status register if the SEND FSM TIMEOUT interrupt cleanup is completed in the handler.

Issue Description: When SEND FSM TIMEOUT interrupt was handled and Frame manager was cleaned, the same MID that was stuck later caused frame mismatch interrupt even before the SEND FSM TIMEOUT interrupt handler is complete. This caused the null check of interrupt status register failure and caused fault 0x5813

Steps To Reproduce: Server power cycle test with MR6.12

ID: SCGCQ01276451 (Port Of Defect SCGCQ01263497)

Headline: SATA only : On EPC feature supported SATA drives, timers are still disabled even after setting the timers using Mode Select command

Description Of Change: In Mode select command power condition translation log page handling for EPC supported drives, the pointer is correctly pointed to SCSI mode select power condition transition page(sent by host) by excluding the header and block descriptor.

Issue Description: When idle timers are enabled using Mode select command with power condition transition(0x1A) log page, timers are not enabled.
When handling translation for EPC supported drives, the pointer referring to the log page data is not pointing to correct location.

Steps To Reproduce: Attach an EPC supported SATA driver, then reboot.

ID: SCGCQ01278488 (Port Of Defect SCGCQ01271703)

Headline: IOP WA:PCIe Config trap on Adv Error Capability and Control Register(Offset 0x118) to disable supporting ECRC checking and generation

Description Of Change: Firmware has to trap any Read or Write to Advanced Error Capability & Control Register (Offset 0x118).
For writes, if bit 8 (Config ECRC Check Enable) and bit 6 (Config ECRC Gen Enable) are ever written to a 1b by the host, dont allow the write to occur to the HW.
For reads firmware should make sure that bit 7 (ECRC Check Capable) and bit 5 (ECRC Generation Capable) are set to zero on the read data back to the host.

Issue Description: In certain conditions, the PCIe hardware logic can incorrectly flag a good TLP as a Malformed TLP. This results in a FATAL error message on PCIe, typically resulting in OS level crash. The workaround is to configure trap on PCIe Config Adv Error Capability and Control register (Offset 0x118) to disable supporting ECRC checking and generation.

Steps To Reproduce: Any good TLP can be flagged as Malformed TLP if the PCIe hardware logic bug is exposed.
Issue reproduced in MegaRaid controller that uses same PCIe hardware chip.

Enhancements Implemented (2):

ID: SCGCQ01174618

Headline: PL : Add Support for PUIS(Power Up In Standby) SATA drives

Description Of Change: PUIS enabled SATA drives get detected when PUIS feature is enabled in controller.

PUIS enabled drives will not spin up when powered on.
Some will spin up with SET FEATURE command and some by sending any media access command.

Since the drive is not spun up, IDENTIFY DEVICE data from the drive will be incomplete.
So firmware has to handle initialization sequence where partial initialization is done and the PUIS drive is exposed to upper layers.
The complete initialization is done once the drive spins up.

ID: SCGCQ01259184 (Port Of EnhancementRequest SCGCQ01244472)

Headline: IOP: MPI FW Upload processing time enhancement

Description Of Change: Firmware is spending unnecessary amounts of time re-validating firmware images when doing an MPI Firmware Upload. This is done so the exact size of a region being uploaded can be returned, which requires re-validation.

Firmware now returns the size of the region itself, and not the image within the region. That significantly reduces the time to execute the FW Upload command, and increases the size of the region data returned to the host, but over all reducing the total time spent executing the MPI FW Upload.

ReleaseOrder ID:	***SCGCQ01281042*** Open In CQWeb
Headline:	***Pre-Alpha Release: SAS3FW_MASTER_DEV - 14.250.01.***
Release Version:	***14.250.01.00***
UCM Project:	***SAS3FW_MASTER_DEV***
Sub UCM Project:	***SAS3FW_Phase15.0***
UCM Stream:	***SAS3FW_MASTER_Invdr_Rel***
Release Type:	***Pre-Alpha***
State:	***Superseded***
Release Baseline:	***SAS3FW_MASTER_DEV-2017-02-21-14.250.01.00_REL_1487664452@ \SAS_CTRL_FW***
Release Date:	***22-FEB-17***
Date Generated:	***Jul 17, 2017***

Defects Fixed (11):

ID: SCGCQ01201578 (Port Of Defect SCGCQ01189751)
Headline: IOP: MCTP: In I2C slave response mode low level errors can have two responses
Description Of Change: Modified the code in the common path for Packet Exceptions to always check for the default response and remove it if the Packet Exception is not the default response.
Issue Description: When MCTP over I2C is configured exclusively as a slave (slave response mode), low level errors like a Packet Integrity Check or PEC (CRC check) failure can have two responses loaded: the Packet Exception (PE) FW In Wrong State and the one just generated. The default response (PE FW In Wrong State) should have been removed.
Steps To Reproduce: Send FW a request with a bad CRC, or cause the bus to corrupt the packet. Perform two I2C reads. The reader will see the first one will be PE FW In Wrong State and the second as PE PEC Failure.

ID: SCGCQ01201579 (Port Of Defect SCGCQ01196986)
Headline: IOP: MCTP: Heavy traffic from host with operations that take a long time can cause controller to stop acknowledging I2C transactions
Description Of Change: Streamlined the interrupt code and modified to reconfigure the I2C hardware to receive an I2C Write when:
1. The I2C byte buffering is not active
2. A start for an I2C write was received
3. Either the I2C write has been stopped or it was NAKed by the I2C hardware

Issue Description: The issue occurs with MCTP over I2C in slave response mode (always an I2C slave).

When heavy traffic with the operations taking a long time occur from a host, particularly multiple MPI FW Upload commands, the firmware can become out of sync with the I2C interrupt handler. Eventually, this leads to firmware no longer receiving interrupts when the I2C hardware receives a new packet because the packets are not being acknowledged. This results in I2C Writes no longer being acknowledged by the controller.
Steps To Reproduce: Run the MCTP I2C in slave response mode and poll on the controller with some command.
Run "sas3flash -c <X> -list" in a loop (at least 6 times), or some other command on the host to generate MPI FW Upload requests.
The MCTP I2C traffic starts seeing acknowledgement errors and the controller stops responding to I2C transactions.

ID: SCGCQ01204905 (Port Of Defect SCGCQ01155407)
Headline: PL fault 5854 seen when system boots with all SATA drives in setup spun down
Description Of Change: Reverted first command for SATA Initialization that was prior to SMR support, where we sent IDENTIFY as the first command, instead of read Block Device Characteristics log page. Rearranged the SATA Initialization sequence to read the Block Device Characteristics log page after the check power mode to avoid checking any initial command failures during SATA initialization.
Issue Description: As part of SMR drive support we had added a new command to read the Block Device Characteristics log page at the start of the SATA Initialization process, replacing the IDENTIFY as the 1st command. We were also not checking for all the errors and command failures of the block device characteristics log page since this was supposed to fail for NON SMR devices. But we also happened to not check for errors related to command not transferred, timeout, drive errors and etc. This lead to further commands sent to drive, though errors were logged in the hardware leading to faults.
Steps To Reproduce: 1. Large configof SATA HDDs. OS on VD on the controller
2. Mark all the PDs Prepare for Removal except OS VD and make sure they are in spundown mode
3. Reboot the server and see if the OS boot fails

ID: SCGCQ01205282 (Port Of Defect SCGCQ01172334)
Headline: PL SATA Only: outstanding SATA passthorugh IO can cause target reset from timer callback check if sata Initialization not done yet
Description Of Change: In timer call back, do not initiate TM immediately if IO is SATA Pass Through command.
Instead initiate TM if the same Passthrough IO still exists even after 4s. Delay initiating TM to make sure IO is stuck.
Issue Description: A SATA Passthrough command issued to a SATA drive requiring initialization results in the controller resetting the SATA drive and failing the passthrough command
Steps To Reproduce: Only issue SATA passthrough IO to SATA drive without any TUR/Report LUN etc.

ID: SCGCQ01220121 (Port Of Defect SCGCQ01219591)
Headline: IOP: MCTP I2C: FW Download sometimes causes controller to be unresponsive
Description Of Change: Modified the I2C receive packet code so that it properly clears out the I2C hardware when multiple I2C packets were missed by the firmware. This code is used when the firmware is trying to receive a new I2C packet.
Issue Description: When an MPI FW Download request is issued to the firmware to update the controller firmware, the I2C interface for MCTP can sometimes become unresponsive. This is because the firmware was not able to process the packets in the I2C hardware while erasing the flash.
Steps To Reproduce: Send an MPI FW Download request.
Continue I2C MCTP operations at the same time.

ID: SCGCQ01221731 (Port Of Defect SCGCQ01150838)
Headline: IOP: MCTP: application sees unexpected severe errors for removed/not registered drives and reset controller
Description Of Change: Controller firmware now sends an MPI SCSI IO reply with IOC Status SCSI Device Not Registered when a device is no longer registered, but a SCSI IO was sent to the device.

When a fault or reset occurs, then disable the MCTP related hardware. This will cause previous I2C bus errors to become I2C address NAK errors.
Issue Description: An MCTP application is seeing severe errors under one of two conditions:
1. A drive is removed or not registered, but a SCSI IO is sent to the drive from the MCTP application before a remove event occurs
- Firmware sends a Command Status Invalid Parameter
2. The controller is under reset, and an I2C bus error occurs when the MCTP application performs and I2C operation it sees bus errors for a a time

Steps To Reproduce: Configure the controller for MCTP over I2C in slave response mode.

For error #1, remove a drive, and then send a SCSI IO to the removed drive through MCTP over I2C.

For error #2, reset or fault the controller, and then send MCTP over I2C traffic tot he controller.

ID: SCGCQ01226356 (Port Of Defect SCGCQ01218943)
Headline: (SATA Only) PL fault 5854 seen when system boots with specific SATA drives spun down
Description Of Change: Block Device Characteristics log page is not supported by many new model drives but is needed to be called to detect if it's SMR or not. In most cases of SATA drives this command fails or times out, even in the case where drives are spun down. So firmware should not be stopping the SATA Initialization for the response from Block Device Characteristics log page , but allow the next set of commands to be sent and allow those commands to stop the SATA Initialization, if needed.
Issue Description: For Spun down SATA drives initial commands during SATA Initialization are completed and firmware also tries to read Block Device Characteristics log page, which fails or times out and thus the command is failed. Some specific bad drives maybe responding post timeout and causing error as the command and context is already freed.
Steps To Reproduce: 1. Connect large number of SATA drives of specific manufacturer to the controller.
2. Spin down all the SATA drives.
3. Reboot the server or reset the controller and observe Fault 0x5854

ID: SCGCQ01259543 (Port Of Defect SCGCQ01041762)
Headline: PL: SAS 3008 controller crash - fault_state(0x584a)
Description Of Change: Modified firmware so we check for this hang condition. When detected, we clear the areas responsible, target reset the device, and continue.
Issue Description: While running stress to all devices in the topology, there exists a possibility in which the data payload of a data frame may be wiped out, but the CRC is still valid. When this occurs, our controller hangs until a timeout condition occurs resulting in a fault.
Steps To Reproduce: 1. Run IO to all devices in the topology.
2. Using a SAS Jammer, inject the following error into the data stream:
   a. Trigger on an incoming data frame.
   b. Remove the data payload from the frame.
   c. re-calculate the CRC, so it is valid

ID: SCGCQ01263737 (Port Of Defect SCGCQ01253195)

Headline: PL Fault 0x5813 caused during SEND FSM TIMEOUT interrupt handling

Description Of Change: Avoided interrupt status register if the SEND FSM TIMEOUT interrupt cleanup is completed in the handler.

Issue Description: When SEND FSM TIMEOUT interrupt was handled and Frame manager was cleaned, the same MID that was stuck later caused frame mismatch interrupt even before the SEND FSM TIMEOUT interrupt handler is complete. This caused the null check of interrupt status register failure and caused fault 0x5813

Steps To Reproduce: Server power cycle test with MR6.12

ID: SCGCQ01276451 (Port Of Defect SCGCQ01263497)

Headline: SATA only : On EPC feature supported SATA drives, timers are still disabled even after setting the timers using Mode Select command

Description Of Change: In Mode select command power condition translation log page handling for EPC supported drives, the pointer is correctly pointed to SCSI mode select power condition transition page(sent by host) by excluding the header and block descriptor.

Issue Description: When idle timers are enabled using Mode select command with power condition transition(0x1A) log page, timers are not enabled.
When handling translation for EPC supported drives, the pointer referring to the log page data is not pointing to correct location.

Steps To Reproduce: Attach an EPC supported SATA driver, then reboot.

ID: SCGCQ01278488 (Port Of Defect SCGCQ01271703)

Headline: IOP WA:PCIe Config trap on Adv Error Capability and Control Register(Offset 0x118) to disable supporting ECRC checking and generation

Description Of Change: Firmware has to trap any Read or Write to Advanced Error Capability & Control Register (Offset 0x118).
For writes, if bit 8 (Config ECRC Check Enable) and bit 6 (Config ECRC Gen Enable) are ever written to a 1b by the host, dont allow the write to occur to the HW.
For reads firmware should make sure that bit 7 (ECRC Check Capable) and bit 5 (ECRC Generation Capable) are set to zero on the read data back to the host.

Issue Description: In certain conditions, the PCIe hardware logic can incorrectly flag a good TLP as a Malformed TLP. This results in a FATAL error message on PCIe, typically resulting in OS level crash. The workaround is to configure trap on PCIe Config Adv Error Capability and Control register (Offset 0x118) to disable supporting ECRC checking and generation.

Steps To Reproduce: Any good TLP can be flagged as Malformed TLP if the PCIe hardware logic bug is exposed.
Issue reproduced in MegaRaid controller that uses same PCIe hardware chip.

Enhancements Implemented (2):

ID: SCGCQ01174618

Headline: PL : Add Support for PUIS(Power Up In Standby) SATA drives

Description Of Change: PUIS enabled SATA drives get detected when PUIS feature is enabled in controller.

PUIS enabled drives will not spin up when powered on.
Some will spin up with SET FEATURE command and some by sending any media access command.

Since the drive is not spun up, IDENTIFY DEVICE data from the drive will be incomplete.
So firmware has to handle initialization sequence where partial initialization is done and the PUIS drive is exposed to upper layers.
The complete initialization is done once the drive spins up.

ID: SCGCQ01259184 (Port Of EnhancementRequest SCGCQ01244472)

Headline: IOP: MPI FW Upload processing time enhancement

Description Of Change: Firmware is spending unnecessary amounts of time re-validating firmware images when doing an MPI Firmware Upload. This is done so the exact size of a region being uploaded can be returned, which requires re-validation.

Firmware now returns the size of the region itself, and not the image within the region. That significantly reduces the time to execute the FW Upload command, and increases the size of the region data returned to the host, but over all reducing the total time spent executing the MPI FW Upload.
