



SCS Engineering Release Notice

ReleaseCandidate Release Version 08.00.00.00 - SAS3FW_MASTER_DEV (SCGCQ00821338)

(SCGCQ00821338) - ReleaseCandidate Release Version 08.00.00.00 - SAS3FW MASTER DEV

(SCGCQ00813738) - Phase8 Beta Release Version 07.250.04.00 - SAS3FW MASTER DEV

(SCGCQ00807601) - Phase8 Alpha Release Version 07.250.03.00 - SAS3FW MASTER DEV

(SCGCQ00802119) - Phase8 Pre-Alpha Release Version 07.250.02.00 - SAS3FW MASTER DEV

(SCGCQ00796319) - Phase8 Pre-Alpha Release Version 07.250.01.00 - SAS3FW MASTER DEV



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Change Summary (Defects=1)

SCGCQ00821128 (DFCT) - Fixed Firmware version to 08.00.00.00



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Total Defects Resolved (1)

(SCGCQ00821128)		Defect 1/1
HEADLINE:	Fixed Firmware version to 08.00.00.00	
DESC OF CHANGE:	Extra 0 in the hex value in version file caused the problem. Corrected it with proper version.	
TO REPRODUCE:	Flash firmware and check version details. It would show wrong version.	
ISSUE DESC:	Firmware version was showing as128.00.00.00, instead of 08.00.00.00	



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Phase8 Beta Release Version 07.250.04.00 - SAS3FW_MASTER_DEV (SCGCQ00813738)

Change Summary (Defects=1)

SCGCQ00807306 (CSET) - PL: Link event codes are not properly converted from hardware to MPI values



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Phase8 Beta Release Version 07.250.04.00 - SAS3FW_MASTER_DEV (SCGCQ00813738)

Total Defects Resolved (1)

(SCGCQ00807306 - Port of SCGCQ00806568)		Defect 1/1
HEADLINE:	PL: Link event codes are not properly converted from hardware to MPI values	
DESC OF CHANGE:	Created defines for hardware event values and used them in the compare.	
TO REPRODUCE:	N/A	
ISSUE DESC:	Some of the link event codes need to be converted from hardware values to MPI values. The check to see which hardware values need to be converted are being compared to MPI values and they should be compared to hardware values.	



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Phase8 Alpha Release Version 07.250.03.00 - SAS3FW_MASTER_DEV (SCGCQ00807601)

Change Summary (Defects=5 Enhancements=2)

SCGCQ00769393 (DFCT) - PL: Enclosure Management SES Diag Page 2 does not check for Generation
Code changes

SCGCQ00785787 (DFCT) - PL: TUR to a SATA command may not return correct ASC/ASCQ

SCGCQ00787481 (DFCT) - IOP: MCTP function only returns failure

SCGCQ00787491 (DFCT) - IOP: Check for failure when DMAing diag buffer strings

SCGCQ00802662 (DFCT) - 'pl sfw' UART/CLI diag command to write a starfish register was broken.

SCGCQ00789106 (CSET) - Shifting of LSI-specific Phy Event Counter encoding

SCGCQ00799344 (CSET) -

Total Defects Resolved (5)**(SCGCQ00769393)** Defect 1/5

HEADLINE: PL: Enclosure Management SES Diag Page 2 does not check for Generation Code changes

DESC OF CHANGE: Added a check for generation code in SES Diag page 2 and it reread the SES diag page 1 if there is a mismatch in SEP generation code.

TO REPRODUCE: Connect an IT controller to an enclosure with an expander and at least a single drive.
Send an MPI SEP Request to a drive attached to the enclosure's expander expander.
Change the enclosure's configuration such that the SES Generation Code changes.
Send another MPI SEP Request to that same drive. Note that the controller does not reread SES Diagnostic Page 1 (Configuration).

ISSUE DESC: The Enclosure Management code that handles MPI SEP Request to an expander reads SES Diagnostic Page 1 (Configuration) the very first time it communicates with the enclosure. It does not reread that page when the Generation Code changes, which is required by SES.

(SCGCQ00785787) Defect 2/5

HEADLINE: PL: TUR to a SATA command may not return correct ASC/ASCQ

DESC OF CHANGE: Added changes in SATL to update sense key and ASC/ASCQ properly.

TO REPRODUCE: Cause a TUR command to a SATA drive to be failed with either the DF bit set, or the ERR bit set and the WP bit not set. The Sense Key and ASC/ASCQ will not be returned correctly.

ISSUE DESC: When a TUR command to a SATA drive is failed with either the DF bit set, or the ERR bit set and the WP bit not set, sense key and ASC/ASCQ are not updated properly.

(SCGCQ00787481) Defect 3/5

HEADLINE: IOP: MCTP function only returns failure

DESC OF CHANGE: The function that handles the default response now has a case to return a success.

TO REPRODUCE: Found by code inspection.

ISSUE DESC: A function that determines whether a default response must be sent only returns failure. This only impacts I2C slave-response mode and when the BMC sends multiple requests with no I2C Read between them. The side effects are not seen externally, and only cause confusion with internal states.

(SCGCQ00787491) Defect 4/5

HEADLINE: IOP: Check for failure when DMAing diag buffer strings

DESC OF CHANGE: Added changes to handle the return status correctly while DMAing diag buffer strings.

TO REPRODUCE: NA

ISSUE DESC: In IOP, while DMAing diag buffer strings the function return status is not handled correctly.

(SCGCQ00802662) Defect 5/5

HEADLINE: 'pl sfw' UART/CLI diag command to write a starfish register was broken.

DESC OF CHANGE: The diag function was previously writing to a invalid address of starfish register. Made it write to the proper location of starfish register.

TO REPRODUCE: Use the uart to WRITE the starfish register with a value. Read back with CLI read and see the difference in values.

ISSUE DESC: When using uart command line to Write to a starfish register, firmware would write to an invalid address.



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Phase8 Alpha Release Version 07.250.03.00 - SAS3FW_MASTER_DEV (SCGCQ00807601)

Total Enhancements Implemented (2)

(SCGCQ00789106 - Port of SCGCQ00769439)

Enhancement 1/2

HEADLINE: Shifting of LSI-specific Phy Event Counter encoding

NEW FUNCTIONALITY: Modified the firmware to retrieve the correct event code for SAS Phy Counter and SAS Phy Page 2 events.

(SCGCQ00799344 - Port of SCGCQ00767971)

Enhancement 2/2



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Phase8 Pre-Alpha Release Version 07.250.02.00 - SAS3FW_MASTER_DEV (SCGCQ00802119)

Change Summary (Defects=3 Enhancements=2)

SCGCQ00787474 (DFCT) - IOP: Poor coding style hides variable

SCGCQ00792742 (DFCT) - PL: Fault 0xD203 observed while releasing Diag Buffer (TRACE)

SCGCQ00795979 (CSET) - Base Address Register at offset 0x1C (BAR3) is writeable when should not be

SCGCQ00791963 (ENHREQ) - SES Page 0Ah Element Index mapping support for enclosure

SCGCQ00792584 (ENHREQ) - NVDATA: Generate SR-IOV .XSD for Fury



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Total Defects Resolved (3)

(SCGCQ00787474) Defect 1/3

HEADLINE: IOP: Poor coding style hides variable
DESC OF CHANGE: Fixed poor coding style which hides variable.
TO REPRODUCE: None
ISSUE DESC: In one of the IOP function, there is a parameter called "Offset" and later a local defined as "Offset"

(SCGCQ00792742) Defect 2/3

HEADLINE: PL: Fault 0xD203 observed while releasing Diag Buffer (TRACE)
DESC OF CHANGE: Added changes to handle the return status while processing DiagBufferPost(TRACE) request.
TO REPRODUCE:

- From host driver send DiagBufferPost(TRACE) request with buffer size equal to 64k.
- From host driver do a DiagBufferRelease(TRACE)
- After release request PL faults with 0xD203.

ISSUE DESC: PL fault 0xD203 is observed when MPI DiagBufferRelease request message is sent from the host driver.

(SCGCQ00795979 - Port of SCGCQ00795305) Defect 3/3

HEADLINE: Base Address Register at offset 0x1C (BAR3) is writeable when should not be
DESC OF CHANGE: Moved code that blocks BAR3 to execute earlier in start-of-day.
TO REPRODUCE: Boot the system. Read BAR3 (offset 0x1C) in the Config Space, and the BAR is available even though it should not be.
ISSUE DESC: During firmware start-of-day there is a small time period where the Base Address Register 3 (BAR3) is available for writing when it should not be.



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Total Enhancements Implemented (2)

(SCGCQ00791963)	Enhancement 1/2
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HEADLINE:	SES Page 0Ah Element Index mapping support for enclosure
NEW FUNCTIONALITY:	Added SES Page 0Ah Element Index mapping support for enclosure for controlling array device elements

(SCGCQ00792584)	Enhancement 2/2
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HEADLINE:	NVDATA: Generate SR-IOV .XSD for Fury
NEW FUNCTIONALITY:	Before the .XSD files were only generated for Invader cards. Now .XSD files are created for the 4 PHY and 8 PHY Fury cards.



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Change Summary (Defects=5 Enhancements=1)

SCGCQ00777858 (DFCT) - PL: In Topology Change Event PhyStatus is not reported as Target Device missing(0x2) upon HDD removal

SCGCQ00789057 (DFCT) - IOP/IR: MCTP: After Volume Creation, no other commands can be executed

SCGCQ00793477 (DFCT) - IOP: Invalid void * arithmetic

SCGCQ00793480 (DFCT) - PL: Possible variable overflow

SCGCQ00788654 (CSET) - PL: Disabling Fast Path can cause memory corruption at start of day

SCGCQ00790308 (ENHREQ) - IOP: Add GPIO Write protect pin feature for SBR EEPROM

Total Defects Resolved (5)

(SCGCQ00777858)		Defect 1/5
HEADLINE:	PL: In Topology Change Event PhyStatus is not reported as Target Device missing(0x2) upon HDD removal	
DESC OF CHANGE:	Added additional code to save the attached device handle when the expander attached drive goes missing.	
TO REPRODUCE:	In the SAS topology, where controller is connected with expander with drives attached to it, remove one of the drives from the expander.	
ISSUE DESC:	When one of drives is removed from the expander phy, PhyStatus 0x2(Target Device is missing) in Topology Change Event is not returned. So that the host driver cannot handle HDD removal properly. Incorrect Attached Device Handle 0x0 is reported.	

(SCGCQ00789057)		Defect 2/5
HEADLINE:	IOP/IR: MCTP: After Volume Creation, no other commands can be executed	
DESC OF CHANGE:	Fixed the boundary conditions for the extended event queue that collects RAID events.	
TO REPRODUCE:	Use storelibtest with SLIR3-MCTP on a BMC with PCIe VDM and create a volume by answering the following storelibtest prompts (with the exception of the drive selection): Enter 1 to Creating PI VD or 0 for Non-PI VD: 0 Do you want to span (Type 'y' for yes)--->n Array ID : 0 Enter number of Physical Drives for array# 0 (1..11)--->2 Enter Physical Drive Index (from PD Summary above)--->0 Enter Physical Drive Index (from PD Summary above)--->1 Enter % size to be used (100% = 570296 MB)--->3 New Logical Drive Count(Max LDs per Array: 1)--->1 Logical Drive 0 RAID Levels (0 1)--->1 NOTE : For the following, to keep the default values, please press ENTER Strip size per DDF for LD 0. Enter a value between [7(64K) - 7(64K)] : [default = stripSize(64K)]---> LD name(Press ENTER for none)---> Disk Cache Policy 1) Unchanged 2) Enable 3) Disable Enter your choice : (default = Unchanged)--->	
ISSUE DESC:	When creating volumes using SLIR3-MCTP and the volume uses 1% of drive capacity, then the controller does not respond to any proceeding MCTP command until a controller reset. This is caused by rush of RAID events, which overflow the extended event queue and effectively disable MCTP on the controller. Only IR is impacted.	

(SCGCQ00793477)		Defect 3/5
HEADLINE:	IOP: Invalid void * arithmetic	
DESC OF CHANGE:	Changed the type of (void *) in accordance with the given arithmetic statement.	
TO REPRODUCE:	NA	
ISSUE DESC:	There are a number of places where FW attempts to do math on a variable with a type of (void *). According to the C and C++ specs, this is illegal.	

(SCGCQ00793480)		Defect 4/5
HEADLINE:	PL: Possible variable overflow	
DESC OF CHANGE:	Typecasted the variable with higher storage class.	
TO REPRODUCE:	Run coverity tool.	
ISSUE DESC:	The variable number of cylinder which is of data type unsigned integer may get overflow due to multiplication with various constants.	



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(SCGCQ00788654 - Port of SCGCQ00783657)

Defect 5/5

HEADLINE:	PL: Disabling Fast Path can cause memory corruption at start of day
DESC OF CHANGE:	Added a check to ensure the correct number of indexes is created, which will prevent PL firmware from looping too many times.
TO REPRODUCE:	Disable fast path by setting the bit in IO Unit Page 1. When firmware starts in this configuration, memory will be written to 0.
ISSUE DESC:	If fast path is disabled globally, PL may subtract 1 from zero and then use the result to clear memory it does not own.



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Total Enhancements Implemented (1)

(SCGCQ00790308)		Enhancement 1/1
HEADLINE:	IOP: Add GPIO Write protect pin feature for SBR EEPROM	
NEW FUNCTIONALITY:	Added a new Write Protect GPIO Function code to handle the write protect feature that may be used on EEPROMs. This is only for the SBR EEPROM.	
