

**ReleaseOrder ID:** DCSG00994481  
**Headline:** GCA Release: IT\_UEFI\_Drv\_Ph20 - 20.00.00.00 UEFI (Signed) BSD  
**Release Version:** 20.00.00.00  
**UCM Project:** IT\_UEFI\_Drv  
**Sub UCM Project:** IT\_UEFI\_Drv\_Ph20  
**UCM Stream:** IT\_UEFI\_Drv\_Ph20\_Rel  
**Release Type:** GCA  
**State:** Released  
**Release Baseline:** IT\_UEFI\_Drv\_Ph20-2021-07-04-20.00.00.00\_REL\_1625411432@\\SAS35  
**Release Date:** 2021-07-04 15:09:51.000000  
**Date Generated:** Jul 14, 2021

## Release History

- [DCSG00994481 - GCA Release: IT\\_UEFI\\_Drv\\_Ph20 - 20.00.00.00 UEFI \(Signed\) BSD](#)
- [DCSG00987530 - Beta Release: IT\\_UEFI\\_Drv\\_Ph20 - 19.255.04.00 UEFI BSD](#)
- [DCSG00973205 - Alpha Release: IT\\_UEFI\\_Drv\\_Ph20 - 19.255.03.00 UEFI BSD](#)
- [DCSG00959456 - Pre-Alpha Release: IT\\_UEFI\\_Drv\\_Ph20 - 19.255.02.00 UEFI BSD](#)
- [DCSG00946493 - Pre-Alpha Release: IT\\_UEFI\\_Drv\\_Ph20 - 19.255.01.00 UEFI BSD](#)

**ReleaseOrder ID:** [DCSG00994481](#) [Open In CQWeb](#)  
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**Sub UCM Project:** IT\_UEFI\_Drv\_Ph20  
**UCM Stream:** IT\_UEFI\_Drv\_Ph20\_Rel  
**Release Type:** GCA  
**State:** Released  
**Release Baseline:** IT\_UEFI\_Drv\_Ph20-2021-07-04-20.00.00.00\_REL\_1625411432@\\SAS35  
**Release Date:** 2021-07-04 15:09:51.000000  
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**ReleaseOrder ID:** [DCSG00987530](#) [Open In CQWeb](#)  
**Headline:** Beta Release: IT\_UEFI\_Drv\_Ph20 - 19.255.04.00 UEFI BSD  
**Release Version:** 19.255.04.00  
**UCM Project:** IT\_UEFI\_Drv  
**Sub UCM Project:** IT\_UEFI\_Drv\_Ph20  
**UCM Stream:** IT\_UEFI\_Drv\_Ph20\_Rel  
**Release Type:** Beta  
**State:** Released  
**Release Baseline:** IT\_UEFI\_Drv\_Ph20-2021-06-22-19.255.04.00\_REL\_1624354620@\\SAS35  
**Release Date:** 2021-06-22 09:36:35.000000  
**Date Generated:** Jul 14, 2021

### Defects Fixed (1):

**ID:** DCSG00975201 (Port Of Defect DCSG00974869)  
**Headline:** UEFI FMP download functions need to check for SEKM enabled bit instead of SEM Capable bit for validation.  
**Description Of Change:** The SEKM feature capable bit check is replaced by SEKM enable bit in FMP validation function.  
**Issue Description:** UEFI FMP download functions need to check for SEKM enabled bit instead of SEM Capable bit for validation. If SEKM is disabled, then this feature is considered to be not present even though the feature capable bit is set.  
**Steps To Reproduce:** 1. Flash a FW which has SEKM capability but its disabled.  
2. Try to flash a non SEKM capable FW on it via FMP.  
3. The FMP does not allow the download.  
4. Since the current FW SEKM is disabled, new FW SEKM feature should not matter for download.

### Enhancements Implemented (1):

**ID:** DCSG00979300 (Port Of EnhancementRequest DCSG00978964)  
**Headline:** Improve build scripts to pack map files in release folder  
**Description Of Change:** Build scripts are improved to zip and put the map files in release folder. This helps for easy download of the map files to store later.

**ReleaseOrder ID:** [DCSG00973205](#) [Open In CQWeb](#)  
**Headline:** Alpha Release: IT\_UEFI\_Drv\_Ph20 - 19.255.03.00 UEFI BSD  
**Release Version:** 19.255.03.00  
**UCM Project:** IT\_UEFI\_Drv  
**Sub UCM Project:** IT\_UEFI\_Drv\_Ph20  
**UCM Stream:** IT\_UEFI\_Drv\_Ph20\_Rel  
**Release Type:** Alpha  
**State:** Released  
**Release Baseline:** IT\_UEFI\_Drv\_Ph20-2021-05-24-19.255.03.00\_REL\_1621872669@\\SAS35  
**Release Date:** 2021-05-24 16:10:29.000000  
**Date Generated:** Jul 14, 2021

### Defects Fixed (2):

**ID:** DCSG00963681  
**Headline:** Out of bound memory is accessed while issuing IOC Init command message  
**Description Of Change:** The proper number of request message frames are allocated and the base address of the pool is sent properly in IOC Init command  
**Issue Description:** The driver while issuing IOCCinit provides base address of the request message frame pool to the firmware and currently it provides an unallocated address for SMID 0. Since SMID 0 is unused no functional issue is seen.  
**Steps To Reproduce:** Code review defect.

**ID:** DCSG00966579 (Port Of Defect DCSG00966401)  
**Headline:** Increase default START STOP UNIT command timeout value from 30 to 120 seconds  
**Description Of Change:** The UEFI BSD reads the BIOS Page1 and uses the SSUTimeout value defined in it for timing SSU commands issued by it. If the page read fails, or if the SSUTimeout value in the page is 0, then the current UEFI BSD assumes a default timeout of 30 seconds, the default timeout value is increased to 120 seconds in this activity.  
**Issue Description:** Currently, the UEFI BSD assumes 30 seconds if BIOS Page1 read fails or the SSUtimeout value is set to zero. Some devices (some large-capacity devices) need more timeout to complete the SSU command. Thus existing 30 seconds need to be increased to 120 seconds to successfully start those drives.

**Steps To Reproduce:** Requires some special drives that require a high timeout value for the SSU command and set the BIOS Page1 SSU timeout value to 0 and observe those drives not getting detected by the UEFI BSD.

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**ReleaseOrder ID:** *DCSG00959456* [Open In CQWeb](#)  
**Headline:** *Pre-Alpha Release: IT\_UEFI\_Drv\_Ph20 - 19.255.02.00 UEFI BSD*  
**Release Version:** *19.255.02.00*  
**UCM Project:** *IT\_UEFI\_Drv*  
**Sub UCM Project:** *IT\_UEFI\_Drv\_Ph20*  
**UCM Stream:** *IT\_UEFI\_Drv\_Ph20\_Rel*  
**Release Type:** *Pre-Alpha*  
**State:** *Released*  
**Release Baseline:** *IT\_UEFI\_Drv\_Ph20-2021-05-03-19.255.02.00\_REL\_1620034396@ISAS35*  
**Release Date:** *2021-05-03 09:32:38.000000*  
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**Enhancements Implemented (1):**

**ID:** DCSG00927211  
**Headline:** UEFI sanity check for VPD page changes in FW.  
**Description Of Change:** UEFI sanity check for VPD page changes in FW. UEFI HII correctly shows the information.

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**ReleaseOrder ID:** *DCSG00946493* [Open In CQWeb](#)  
**Headline:** *Pre-Alpha Release: IT\_UEFI\_Drv\_Ph20 - 19.255.01.00 UEFI BSD*  
**Release Version:** *19.255.01.00*  
**UCM Project:** *IT\_UEFI\_Drv*  
**Sub UCM Project:** *IT\_UEFI\_Drv\_Ph20*  
**UCM Stream:** *IT\_UEFI\_Drv\_Ph20\_Rel*  
**Release Type:** *Pre-Alpha*  
**State:** *Released*  
**Release Baseline:** *IT\_UEFI\_Drv\_Ph20-2021-04-12-19.255.01.00\_REL\_1618219300@ISAS35*  
**Release Date:** *2021-04-12 09:21:17.000000*  
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**Defects Fixed (1):**

**ID:** DCSG00937946 (Port Of Defect DCSG00937188)  
**Headline:** The SSU timeout value specified in HBA's configuration settings is ignored.  
**Description Of Change:** The BSD is reading HBA's configuration data using end point device's handle. This always results in Invalid Handle. Thus SSU timeout value is ignored. Using HBA's handle correctly reads the configuration data.  
**Issue Description:** SSU Timeout value specified in configuration is ignored by BSD. BSD always uses default timeout value which is 30 seconds.  
**Steps To Reproduce:** - Connect some end point devices which need device spin up command (SSU) during HBA initialization.  
- Set 45 seconds as SSU timeout seconds in configuration data.  
- Check that BSD actually waits for 45 seconds for SSU command.  
- BSD is always timing out at 30 seconds for SSU command.

**Enhancements Implemented (1):**

**ID:** DCSG00520482  
**Headline:** The UEFI Driver should manage the controller only if it is loaded from the controller.  
**Description Of Change:** The UEFI Driver should manage the controller only if it is loaded from the controller. This is achieved by comparing controller's handle device path with the driver's loaded images device path. If they are same (excluding media relative offset) then driver is said to be loaded from same controller device. If they are different then Supported function will return UNSUPPORTED.  
Note: The driver must be loaded from device's flash during system boot for this feature to work.

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