BROADCOM Release Notes: GCA Release: CtrlFw_Ph_21.0 - 21.00.00.00 Firmware

ReleaseOrder ID:	*DCSG01061106*
Headline:	*GCA Release: CtrlFw_Ph_21.0 - 21.00.00.00 Firmware*
Release Version:	*21.00.00.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_21.0*
UCM Stream:	*CtrlFw_Ph_21.0_Rel*
Release Type:	*GCA*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_21.0-2021-10-14-21.00.00.00_REL_1634217286@ \SAS35*
Release Date:	*2021-10-14 13:12:39.000000*
Date Generated:	*Oct 21, 2021*

Release History

- DCSG01044604 - ReleaseCandidate Release: CtrlFw_Ph_21.0 - 20.250.09.00 Firmware
- DCSG01040824 - Beta Release: CtrlFw_Ph_21.0 - 20.250.08.00 Firmware
- DCSG01035679 - Beta Release: CtrlFw_Ph_21.0 - 20.250.07.00 Firmware
- DCSG01034047 - Alpha Release: CtrlFw_Ph_21.0 - 20.250.06.00 Firmware
- DCSG01029038 - Alpha Release: CtrlFw_Ph_21.0 - 20.250.05.00 Firmware
- DCSG01015805 - Alpha Release: CtrlFw_Ph_21.0 - 20.250.04.00 Firmware
- DCSG01010059 - Pre-Alpha Release: CtrlFw_Ph_21.0 - 20.250.03.00 Firmware
- DCSG01006336 - Pre-Alpha Release: CtrlFw_Ph_21.0 - 20.250.02.00 Firmware
- DCSG00996118 - Pre-Alpha Release: CtrlFw_Ph_21.0 - 20.250.01.00 Firmware

ReleaseOrder ID:	*DCSG01044604* Open In CQWeb
Headline:	*ReleaseCandidate Release: CtrlFw_Ph_21.0 - 20.250.09.00 Firmware*
Release Version:	*20.250.09.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_21.0*
UCM Stream:	*CtrlFw_Ph_21.0_Rel*
Release Type:	*ReleaseCandidate*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_21.0-2021-09-21-20.250.09.00_REL_1632244352@\SAS35*
Release Date:	*2021-09-21 17:10:50.000000*
Date Generated:	*Oct 21, 2021*

Defects Fixed (1):

ID: DCSG01041327
Headline: Added "TimeSyncInterval" to the FW ManPage11 data-struct to match the XSD definition
Description Of Change: - Updated ManPage11 data-struct within the FW to include the "TimeSyncInterval" member which is used by the driver to sync the host-time-stamp with the FW
- This member is not used by the FW and this change does not affect any FW functionality
- The data-struct was updated to keep the FW in sync with the XSD definitions
Issue Description: - During the original ER implementation, the XML/XSD files were updated to include the "TimeSyncInternal" for the driver
- Since this field is not used by the FW, the FW data-struct was not updated
Steps To Reproduce: - Review the code to match the ManPage11 definition from XSD with the FW definition

ReleaseOrder ID:	*DCSG01040824* Open In CQWeb
Headline:	*Beta Release: CtrlFw_Ph_21.0 - 20.250.08.00 Firmware*
Release Version:	*20.250.08.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_21.0*
UCM Stream:	*CtrlFw_Ph_21.0_Rel*
Release Type:	*Beta*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_21.0-2021-09-17-20.250.08.00_REL_1631871001@ \SAS35*
Release Date:	*2021-09-17 09:28:46.000000*
Date Generated:	*Oct 21, 2021*

Defects Fixed (1):

ID: DCSG01038387 (Port Of Defect DCSG00987835)
Headline: Aero 7.19 iMR: CBB unable to find secondary image
Description Of Change: For MR-only CBB build, pass the flash base of the APP image found/booted to MR, for dual image iMR support.
Issue Description: MR can't boot to APP image in secondary position, so MR CBB needs to pass the flash base to MR so that it can use the appropriate image.
Steps To Reproduce: Flash attached files, 32mb first, then storcli flash the nopad and reboot.

ReleaseOrder ID:	*DCSG01035679* Open In CQWeb
Headline:	*Beta Release: CtrlFw_Ph_21.0 - 20.250.07.00 Firmware*
Release Version:	*20.250.07.00*
UCM Project:	*CtrlFw*
Sub UCM Project:	*CtrlFw_Ph_21.0*
UCM Stream:	*CtrlFw_Ph_21.0_Rel*
Release Type:	*Beta*
State:	*Released*
Release Baseline:	*CtrlFw_Ph_21.0-2021-09-09-20.250.07.00_REL_1631188056@ \SAS35*
Release Date:	*2021-09-09 11:45:27.000000*
Date Generated:	*Oct 21, 2021*

Defects Fixed (2):

ID: DCSG01030777
Headline: SATA only : ATA PT command for SMART READ ATTRIBUTE THRESHOLDS(B0h/D1h) fail when COUNT field is set to 0
Description Of Change: Set the datalenth to 512bytes when ATA PT command for SMART READ ATTRIBUTE THRESHOLDS(B0h/D1h) is sent.
Issue Description: SMART READ ATTRIBUTE THRESHOLDS(B0h/D1h) fails when COUNT field is set to 0.
As per ATA ACS, COUNT field is not applicable and transfer length is fixed to 512bytes.
Steps To Reproduce: Issue ATA PT command for SMART READ ATTRIBUTE THRESHOLDS(B0h/D1h) with COUNT field set to 0

ID: DCSG01032601 (Port Of Defect DCSG01032600)
Headline: SPDM key reading failed when complete flash Erase case
Description Of Change: MPI26_SEC1_CONSUMER_DEVICE_KEY macro value changed from 0x3 to 0x0 in the latest MPI release. Reverted to the actual value
Issue Description: Observing SPDM key pair reading failure when complete flash erase case.
Steps To Reproduce: Test case:
1. Erase all
2. Load Ph16 firmware and it will generate the key pair.
3. Upgrade to PH20 and here kay pair reading is failed.

Enhancements Implemented (2):

ID: DCSG00966563
Headline: Update linker script file for mbed TLS component
Description Of Change: Update linker script file for mbed TLS Library

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ID: DCSG01032931 (Port Of EnhancementRequest DCSG00980247)
Headline: Sea iMR CBB Updates
Description Of Change: Allow MR CBB to boot without True Random Number Generator.

ReleaseOrder ID: ***DCSG01034047*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_21.0 - 20.250.06.00 Firmware***
Release Version: ***20.250.06.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_21.0***
UCM Stream: ***CtrlFw_Ph_21.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_21.0-2021-09-07-20.250.06.00_REL_1631026243@\SAS35***
Release Date: ***2021-09-07 14:50:00.000000***
Date Generated: ***Oct 21, 2021***

Defects Fixed (3):

ID: DCSG00500454
Headline: Trigger script with PassComponentTable Command set to invalid Value led to rolling PLDM error messages
Description Of Change: During PLDM FW update is in progress, FD shall reply to the cancel update/cancel update component command with completion code BUSY_IN_BACKGROUND in case FD is waiting for a response from UA.
Issue Description: - When the PLDM FW update is in progress and till transfer complete stage we got the response from UA/Script.
- once FW completes the Verify image, FW allocates the request frame and sent the details to UA .
- As per the design, The request Frame allocated by FW gets freed as soon as FW receives the response from the UA for Verify complete.
- But FW did not receive the response for Verify complete instead UA sent a new request to cancel the FW update.
- Due to this FW never freed the request frame allocated during the verify complete stage and causes subsequent request frame allocation failures
Steps To Reproduce: - User Initiate PLDM Firmware Update script which has unexpected response code sent during Transfer complete state.
- Script ends at Transfer complete stage once the validation completes and sends the cancel update to make sure FW moves to Idle state.
- User initiate another PLDM FW update to inject error response code at different stage of PLDM FW update state machine.
- When FW update starts, Observed that the request message frame allocation failures continuously.

ID: DCSG01023749 (Port Of Defect DCSG01021656)
Headline: Fault 0xEC0F seen while aborting an active recovery on a NVMe drive
Description Of Change: Remove the timed NVMe admin command from the PL timer bucket and reset the timer used for NVMe capability Timeout during an abort.
Issue Description: The NVMe recovery toolbox command when aborted, the timed Admin IO was neither removed from the PL timer bucket nor the timer used for accuracy was reset.
Steps To Reproduce: Issue an abort to an ongoing toolbox NVMe recovery command.

ID: DCSG01032306 (Port Of Defect DCSG01026871)
Headline: Incorrect usage of Block Limits Virtual physical disk npwg field resulting in 0x7 being treated as 7 512B sector length IOs with NVMe drives
Description Of Change: Incremented the NVMe NPWG field by 1 before writing into the SCSI NOWS field.
Issue Description: One field was zero based and the other was 1 based.
Steps To Reproduce: Run small random writes or reads using 16 direct attached (x1) vendor CM6-V NVMe drives and measure iops. Results are limited to ~3.5M iops and 2.5M iops for reads and writes respectively. We are able to achieve ~6.6M iops and ~5.2M iops with these drives in linux, and in windows when single drive raid 0 volumes are created.

Enhancements Implemented (4):

ID: DCSG00948894
Headline: [Aero][BST] Improve the code coverage by adding new test cases
Description Of Change: 1. Add test case to hot plug Expander attached to controller (Within DMD and After DMD expires)
2. Add test case to Send IOUnitControl Command to clear error counters.

ID: DCSG00949307
Headline: [BST] Add SEP related test cases
Description Of Change: Added BST script to send locate on/off to all the attached drives.

ID: DCSG00999219
Headline: BST CodeCoverage : Add BST test case to improve MPI task management code coverage
Description Of Change: Modified task management BST script to send task management to MPI attached device.

ID: DCSG01027037
Headline: [BST] Graceful handling of controller reset scenario
Description Of Change: 1. Added wrapper API to do controller reset. This API will check if the controller reset is disabled before executing controller reset. If it is disabled, then it will enable controller reset, execute controller reset and disable it back.
2. Replaced controller reset call with the newly added wrapper API in all BST scripts.
3. Start of BST execution, enabled controller reset for all controllers.

ReleaseOrder ID: ***DCSG01029038*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_21.0 - 20.250.05.00 Firmware***
Release Version: ***20.250.05.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_21.0***
UCM Stream: ***CtrlFw_Ph_21.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_21.0-2021-08-30-20.250.05.00_REL_1630338234@\SAS35***
Release Date: ***2021-08-30 15:43:16.000000***
Date Generated: ***Oct 21, 2021***

Defects Fixed (2):

ID: DCSG01025293
Headline: (SATA Only) Inquiry command to read Block device Characteristics VPD Page fails on some SATA drives
Description Of Change: Added a check to see if the SATA drive supports ACS 3 or ACS 4 before sending the command to read the Supported Capabilities log page.
Issue Description: To populate all fields of the Block Device Characteristics VPD Page for SATA drive. Firmware reads the Identify data and Supported Capabilities log page. Some old drives do not support the Supported Capabilities log page so command to read the page is aborted by the drive and this leads to Inquiry command getting failed.
Steps To Reproduce: Attach an old SATA drive to the controller and send an Inquiry command to read the Block Device Characteristics VPD Page (0xB1) to the SATA drive.

ID: DCSG01028477
Headline: No Default value of DMA FIS Timeout
Description Of Change: In case DMA FIS Timeout value is not programmed in NVDATA, a default value of 2 seconds is used.
Issue Description: DMA FIS Timeout value is set in NVDATA in updated manufacturing page 11, however in case the manufacturing page is not updated in old NVDATA it sets the timeout as 0 which results in multiple IO failures.
Steps To Reproduce: Flash the latest firmware with old NVDATA where manufacturing page 11 is not updated to include DMA FIS timeout value.

Enhancements Implemented (2):

ID: DCSG00977495
Headline: Reintroduces the previous security page as MR_MPI26_CONFIG_PAGE_SECURITY_1 to align with current NVDATA
Description Of Change: SPDM security page definitions are changed associated with revision 2.6.11. With these changes, SPDM functionality is broken.
Certificate and key pair reading also failed.
So reverting to old definitions same as Ph16.

ID: DCSG01017044
Headline: Code Space Optimization
Description Of Change: Removed unused functions for code space optimization.

ReleaseOrder ID: ***DCSG01015805*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_21.0 - 20.250.04.00 Firmware***
Release Version: ***20.250.04.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_21.0***
UCM Stream: ***CtrlFw_Ph_21.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_21.0-2021-08-11-20.250.04.00_REL_1628697525@\SAS35***
Release Date: ***2021-08-11 15:58:01.000000***
Date Generated: ***Oct 21, 2021***

Defects Fixed (3):

ID: DCSG00984134
Headline: ScrutinyCLI in UEFI mode failed to download Aero MR NOPAD images using hostboot (hb) command
Description Of Change: MR layout used by CBB was not updated when MR FW APP went from 4 MB to 5 MB in size, this has now been fixed.
Issue Description: Customer is trying to hostboot aero MR NOPAD image and try to flash NOPAD image encounter failure.

After SE debug:
ScrutinyCLI is sending NOPAD image file (via doorbell after validating its signature successfully) to download NOPAD image, but since MR fw download operation does not understand this NOPAD image, so MR fw replying invalid field type (0x7 =MPI2_IOCSTATUS_INVALID_FIELD) from its download operation function.

DEBUG: maskedIOCStatus = 0 . IOCStatus = 0, IOCLogInfo = 0
DEBUG: maskedIOCStatus = 0 . IOCStatus = 0, IOCLogInfo = 0
DEBUG: maskedIOCStatus = 7, IOCStatus = 7, IOCLogInfo = 0 <= (0x7 =MPI2_IOCSTATUS_INVALID_FIELD)
ERROR: Firmware download failed for image type component
DEBUG: ERROR CODE 02020003
Steps To Reproduce: scrutiny.efi -i 2 hb -pkg <pkg file>

ID: DCSG01012204
Headline: Update the Default Vendor ID of Virtual SES Device
Description Of Change: Updated default Vendor ID of Virtual SES Device to "BROADCOM"
Issue Description: Currently default Vendor ID of Virtual SES Device is "LSI"
Steps To Reproduce: 1. Create Debug FW to fail the Man Page 46 config page read request while build inquiry data for vSES device
2. Send Inquiry command to vSES device

ID: DCSG01012237
Headline: BST: Fix scripts for SAL stability.
Description Of Change:
Disabled test case causing exception during test run.
Issue Description:
Exception was observed during BST.
Steps To Reproduce:
Execute BST job.

Enhancements Implemented (2):

ID: DCSG01010542
Headline: BST: Update boardnames in configuration data
Description Of Change:
Updated Boardname in BST scripts.

ID: DCSG01015478
Headline: Remove allocation of PCIe devices when NVMe is disabled in NVDATA
Description Of Change: When the manufacturing page 9 flags field has the NVMe enabled bit cleared, set the PCI drives and switches allocated devices to 0.

ReleaseOrder ID: ***DCSG01010059*** Open In CQWeb
Headline: ***Pre-Alpha Release: CtrlFw_Ph_21.0 - 20.250.03.00 Firmware***
Release Version: ***20.250.03.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_21.0***
UCM Stream: ***CtrlFw_Ph_21.0_Rel***
Release Type: ***Pre-Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_21.0-2021-08-02-20.250.03.00_REL_1627908449@\SAS35***
Release Date: ***2021-08-02 12:46:56.000000***
Date Generated: ***Oct 21, 2021***

Defects Fixed (2):

ID: DCSG00947451
Headline: FW Fault 2622 observed during system boot up in some new Gen4/Gen5 servers
Description Of Change: Disabled the hardware workaround (for Aero) that enabled the hardware core interrupt causing this fault.
Issue Description: An unhandled hardware core interrupt is generated during boot up, this results in firmware fault with fault code 0x2622. This interrupt was enabled due to a hardware workaround, but this hardware bug is only applicable to Ventura controllers.
Steps To Reproduce: Attach a few drives to the Aero controller in a latest Gen 4/Gen 5 server. Boot up the system and observe that firmware fault with fault code 0x2622.

ID: DCSG00972342
Headline: [Aero] PCIe Compliance Configuration Failure - 1_44 DPA Ext Cap Struct
Description Of Change: Increasing the max latency time of DPA state transition from 500ms to 1000ms.
Applications will now wait for 1000ms before reading the DPA registers
Issue Description: PCIE Test compliance application resets the HBA and writes to DPA registers and Read back.
Write to DPA register immediately after reboot takes more than the current 500ms as initial boot code gets more priority.
Application tries to read before the actual write is completed and consider the test as failure.
Steps To Reproduce: Run the PCIE compliance test.

Enhancements Implemented (4):

ID: DCSG00947724
Headline: [Aero][BST] Improve the code coverage of file plPciDeviceManager.c
Description Of Change: Hot removal and addition of PCIe switch and Nvme devices
Disable PCIe phys to remove switch and enable back to add the switch back.

ID: DCSG00949284
Headline: Code Coverage improvement for managed switch SES stack
Description Of Change:
Added test cases to read SES pages for all enclosure devices.

ID: DCSG00949285
Headline: Code Coverage improvement for managed switch MPI device stack
Description Of Change:
Added test cases to trigger MPI dveice state machine for various states.

ID: DCSG00985842
Headline: BST: Add custom Cardnames to BST UART configuration
Description Of Change:
Update BST UART configuration with custom cards.

ReleaseOrder ID: ***DCSG01006336*** Open In CQWeb
Headline: ***Pre-Alpha Release: CtrlFw_Ph_21.0 - 20.250.02.00 Firmware***
Release Version: ***20.250.02.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_21.0***
UCM Stream: ***CtrlFw_Ph_21.0_Rel***
Release Type: ***Pre-Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_21.0-2021-07-26-20.250.02.00_REL_1627296450@\SAS35***
Release Date: ***2021-07-26 10:46:49.000000***
Date Generated: ***Oct 21, 2021***

Defects Fixed (3):

ID: DCSG00995519
Headline: RefClk enabled for sgpio backplane type
Description Of Change: Do not enable PCIe refclk for SGPIO BP
Issue Description: PCIe reference clock gets enabled for downstream devices on an SGPIO backplane.
Steps To Reproduce: 1) Connect a SGPIO BP to Aero HBA.
2) Observe that PCIe refclk is sent to SGPIO BP.

ID: DCSG00996085 (Port Of Defect DCSG00991409)
Headline: Some drives missing in OS when Direct attached slot order event replay flag is set in NVDATA
Description Of Change: Set the correct starting phy of the port when the function to send the SAS topology change list event is called during event replay for the direct attached slot order case.
Issue Description: For direct attached slot order event replay, the ports are arranged in order of slot numbers. Then SAS Topology change list events are sent for ports in order.

There was an issue with multi VSes configuration where a wrong enclosure handle could be set for some phys of the port. To resolve this the SAS Topology change list event for the port was split into multiple events based on phys of a port belonging to different enclosures. To achieve that, a 'starting phy' common between first enclosure and port was sent to the function sending the event, which then returns the last phy of that enclosure. Same is repeated for next enclosure.

However there was a bug in the fix where on moving to next port the starting phy was set 0 instead of actual first phy of the port.
Steps To Reproduce: Attach three or more SAS/SATA drives directly to the controller and set the NVDATA flag to enable direct attached slot order event replay.

ID: DCSG01003869 (Port Of Defect DCSG00995575)
Headline: Connector name in SAS Device Page 0 of the VSes/DA-SEP is not set correctly
Description Of Change: Use the enclosure attached phy to get the phy index for VSes or DA-DEP device instead of using the Port.
Issue Description: To fill the Connector Name field of the device, its Port is used to get the controller phy index the device is connected to. Connector Name is then filled using the phy index in the the Connector Info structure of the Manufacture page 7.
In case of VSes or DA-SEP devices a default port Port 0 is used. In case there is no end device connected to Port 0, this can result in some junk values being filled in the Connector Name field of the SAS device page 0.
Steps To Reproduce: Read the SAS Device Page 0 of the VSes or DA-SEP device when there is no drive connected to phy 0 to 7 of the controller.

Enhancements Implemented (1):

ID: DCSG00999763
Headline: ATA Passthrough handling of ATA commands(PIO DATA IN) obsolete in latest ATA specification for backward compatibility
Description Of Change: When the below set of PIO DATA IN commands that are obsolete in latest spec are issued as ATA PT command, set the datalenght to 512 bytes.
CFA TRANSLATE SECTOR - 87h, PIO Data-In
DEVICE CONFIGURATION IDENTIFY - B1h/C2h, PIO Data-In
IDENTIFY PACKET DEVICE - A1h, PIO Data-In
SMART READ DATA - B0h/D0h, PIO Data-In

As per ATA ACS specification(older version ACS2), the COUNT filed is NA.
Irrespecitive of the count field, drive will transfer 512 bytes of data.

ReleaseOrder ID: ***DCSG00996118*** Open In CQWeb
Headline: ***Pre-Alpha Release: CtrlFw_Ph_21.0 - 20.250.01.00 Firmware***
Release Version: ***20.250.01.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_21.0***
UCM Stream: ***CtrlFw_Ph_21.0_Rel***

Release Type: ***Pre-Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_21.0-2021-07-07-20.250.01.00_REL_1625659167@\SAS35***
Release Date: ***2021-07-07 11:58:51.000000***
Date Generated: ***Oct 21, 2021***

Defects Fixed (2):

ID: DCSG00989522 (Port Of Defect DCSG00986779)
Headline: Incorrect slot number reported for drive with bad Phy
Description Of Change: The fix for this issue will be done in managed switch firmware and PL firmware. In the PL firmware change is made to ensure that PL firmware will not overwrite the value of "Invalid" Field in SES Page 0Ah descriptor coming from managed switch firmware for drives connected behind managed switch.
Issue Description: The SES Page Descriptor 0Ah has the invalid bit set for this slot and MR firmware reports element index as the slot information instead of slot number for this slot while reporting bad Phy.
Steps To Reproduce: 1. Induce bad Phy by taping the drive.
2. Check the AEN and corresponding "physical drive slot" it is indicating.

ID: DCSG00990809 (Port Of Defect DCSG00969750)
Headline: PCIE failure causes TBM failure which leads to control plane hang
Description Of Change: Ensure faster transition to WFI for the hot reset and faulting cases
Alter the RMC reset state machine such that the order in which things are shut down prevents the SAS hang
Add a check before every trace post for the PCIe error and fault if it is in a failed state to avoid prints
Also disable trace posts until the chip is reset
Issue Description: In a tests wherein the driver is running and an ungraceful shutdown with BME clear and Hot Reset is performed in a loop, once ever 100 times the RMC and A15 freeze causing the PCIe interface to fail responding to config cycles after the hot reset completes on the bus.
Clearing the BME causes PCIe errors internal to the chip which are propagated to DMA interfaces including TBM (Trace Buffer Manager)
When the TBM fails a buffer flush it will freeze up the bus if more than 1 write is made to the buffer trace registers
The reset algorithm also indicates that the SAS core was hanging due to this activity
Steps To Reproduce: Create a script which loops on the following
1) Load a VM which boots far enough that the in-box Linux driver is initialized and talking to many drives (raw drives)
2) Have the Hypervisor ungracefully shut down the VM by clearing BME and then issuing a Hot Reset within microseconds of each other without warning or shutdown.
3) AFter the hot reset training sequence have the Hypervisor send over 8 config requests
4) Loop on 1-3 until the system PSODs

Enhancements Implemented (2):

ID: DCSG00952761
Headline: Add NVDATA option to change DMA Activate FIS timeout value.
Description Of Change: Added a field in manufacturing page 11, which is used to set the DMA Activate FIS timeout value in hardware register.

ID: DCSG00961958
Headline: Add partial xml for 9502-16i Controller OCP form factor
Description Of Change: Added partial xml for 9502-16i controller based on 9500-16i partial xml.
Updated the PNP ID
Vendor: 0x1000 Dev: 0x00E6 SubVendor: 0x1000 SubDev: 0x40C0