BROADCOM Release Notes: GCA Release: CtrlFw_Ph_19.0 - 19.00.00.00 Firmware

ReleaseOrder ID: *DCSG00952264*
Headline: *GCA Release: CtrlFw_Ph_19.0 - 19.00.00.00 Firmware*
Release Version: *19.00.00.00*
UCM Project: *CtrlFw*
Sub UCM Project: *CtrlFw_Ph_19.0*
UCM Stream: *CtrlFw_Ph_19.0_Rel*
Release Type: *GCA*
State: *Released*
Release Baseline: *CtrlFw_Ph_19.0-2021-04-21-19.00.00.00_REL_1619017914@\SAS35*
Release Date: *2021-04-21 15:11:16.000000*
Date Generated: *Apr 26, 2021*

Release History

ReleaseOrder ID: *DCSG00930429* Open In CQWeb
Headline: *ReleaseCandidate Release: CtrlFw_Ph_19.0 - 18.250.05.00 Firmware*
Release Version: *18.250.05.00*
UCM Project: *CtrlFw*
Sub UCM Project: *CtrlFw_Ph_19.0*
UCM Stream: *CtrlFw_Ph_19.0_Rel*
Release Type: *ReleaseCandidate*
State: *Released*
Release Baseline: *CtrlFw_Ph_19.0-2021-03-19-18.250.05.00_REL_1616159374@\SAS35*
Release Date: *2021-03-19 13:08:56.000000*
Date Generated: *Apr 26, 2021*

Defects Fixed (3):

ID: DCSG00788430
Headline: Fault 0x7600 observed when 1 phy is disabled in SAS IO Unit page 1
Description Of Change: Set a flag indicating that port configuration failed due to wrong SAS IO Unit page 1. If this flag is set mark the discovery complete and fail port enable to host.
Issue Description: If PCIe IO Unit page 1 is programmed with more than 1 phy in same PCIe link, then it is not allowed to disable only one of those phys in SAS IO Unit page 1. During port enable firmware detects this condition and fails port initialization if SAS IO Unit page 1 is wrongly programmed. However the discovery continues and might fault since ports are not initialized.
Steps To Reproduce: Program the SAS IO Unit page 1 such that only 1 of the phy part of a PCIe link is disabled, then connect few direct attached drives to the controller. Fault 0x7600 is observed during port enable.

ID: DCSG00918020
Headline: Ventura/Mercator: pl: 4311 fault
Description Of Change: Added an interlock between PCIe link down/hot reset hardware cleanup and SAS/SATA hybrid protocol mode selection to prevent the latter from attempting to change one or more phys' protocol modes while the former has placed the phy hardware in reset.
Issue Description: If both SAS/SATA and PCIe modes are enabled on device side phys and a backplane, cable, or SAS/SATA device is attached that causes PCIe receiver detection to succeed even though no PCIe device is attached, the PCIe and SAS/SATA subsystems may have an unexpected interaction that causes a 4311 fault.
Steps To Reproduce: Configure device side phys for mixed SAS/SATA/PCIe mode. Connect a backplane and SAS/SATA devices with the described property and boot the HBA.

ID: DCSG00927932 (Port Of Defect DCSG00925970)
Headline: Bad PHY events generated by RAID stack for invalid VSES elements slot with Critical status
Description Of Change: Added checks in PL to ensure element status code (Critical-2h) for I2C access error is populated only for the UBM array device elements managed by the current VSES.
Issue Description: VSES reports UBM backplane I2C access failures through SES status diag page 02h Element Status Code (Critical 2h) of the associated Array Device Slot Elements. When I2C access error is observed on a UBM connector that is not managed by the current VSES, PL incorrectly populates elements status code to critical for unmanaged elements of the current VSES. The behavior follows for the other VSES device in a multi-VSES config. This causes RAID stack to generate Bad Phy events for invalid VSES elements slot.
Steps To Reproduce: Attach RAID HBA to OEM dual UBM backplane config and boot to UEFI Shell. Perform UBM backplane FW update.
After sometime observe "EVT#00562-03/05/21 13:43:00: 185=Enclosure PD 86(c None/p1) Phy bad for slot XX" messages for invalid VSES Enclosure slots.

Enhancements Implemented (1):

ID: DCSG00930106
Headline: Create Partial XML for 9502-16e HBA
Description Of Change: Added partial XMLs for the 9502-16e HBA based on 9500-16e. SAS/SATA Profile and Mixed profile for 16 NVMe drives added to nvdata folder.

ReleaseOrder ID: *DCSG00921608* Open In CQWeb
Headline: *Alpha Release: CtrlFw_Ph_19.0 - 18.250.04.00 Firmware*
Release Version: *18.250.04.00*
UCM Project: *CtrlFw*
Sub UCM Project: *CtrlFw_Ph_19.0*
UCM Stream: *CtrlFw_Ph_19.0_Rel*
Release Type: *Alpha*
State: *Released*
Release Baseline: *CtrlFw_Ph_19.0-2021-03-03-18.250.04.00_REL_1614771923@\SAS35*
Release Date: *2021-03-03 11:44:26.000000*
Date Generated: *Apr 26, 2021*

Defects Fixed (8):

ID: DCSG00335615
Headline: SPDMLIB: Reduce number of arguments passed to IT FW debug print functions
Description Of Change: Trim down debug print message argument to 4 or less in SPDM LIB to support IT FW debug print function.
Issue Description: New debug print messages added in SPDM LIB with more than 4 arguments which exceeds number of print arguments (4) allowed in IT FW.
Steps To Reproduce: Run BMC Emulator Attestation test on IT card.

ID: DCSG00335755
Headline: MBEDTLSLIB: Compile out Mbed TLS Self-Test code
Description Of Change: Mbed TLS SelfTest code is not needed at this time, so we undefine SelfTest code to save some code space.

Issue Description: Mbed TLS SelfTest code is not needed at this time, so we undefine SelfTest code to save some code space.

Steps To Reproduce: Review the build map file and see SelfTest code is enabled.

ID: DCSG00381441

Headline: Enclosure handle for some direct attached device might be wrong during Event replay for direct attached slot order case.

Description Of Change: While sending SAS topology change list event for a port filter the phys based on enclosure handle they belong to. Send multiple events if the phys of the port belong to different enclosure handles.

Issue Description: In direct attached slot order event replay case, all the ports are arranged in order of their slot number.
Then for each port a SAS topology change list event is sent for all phys within that port. The enclosure handle used for this event is the enclosure handle of the first phy of the port.
However in multi-VSES case where the sets of 4 phys are connected to different types of backplanes and only one drive is connected to phy 4-7, then all phys are in default port 0 but the enclosure handle for phy 0-3 and 4-7 is different.

Steps To Reproduce: Connect phys 4-7 to a UBM backplane with one SAS/SATA drive and don't connect phys 0-3 to any backplane. Notice the enclosure handle for device add event sent for the device in UBM to be incorrect.

ID: DCSG00547436

Headline: SPDM Authentication fails when BMC re-triggers SPDM Handshake

Description Of Change: In Get Version command handling in SPDM LIB, added a check if certificate buffer list is not empty when this command is received, clear out buffer list to clear any residual certificate data in the buffer. This will prevent any old certificate data from contributing to M1 computation for current Challenge command.

Issue Description: OEM BMC had out of date security root certificate in its Trust Store and controller card had updated security certificate, when this root certificate on BMC was removed and updated root certificate was added, BMC re-triggered SPDM handshake operations couple of times, but BMC failed Challenge due to signature verification failed on last Challenge command.

Steps To Reproduce: 1) Have a controller card with latest security certificate

2) Add a dummy root certificate or out of date root certificate to BMC Trust Store

3) From BMC, remove dummy or out of date root certificate, and add an updated and correct root certificate to BMC Trust Store. This will re-trigger SPDM handshake operations at least couple of time and BMC would fail the last Challenge command for signature verification fail.

ID: DCSG00758163

Headline: Fault 0x070A observed while performing firmware downgrade.

Description Of Change: Increased the firmware timer that waits for controller reset after firmware download to 21 seconds.

Issue Description: In firmware downgrade case after the firmware image download is complete, the firmware starts a timer where it waits for up to 10 seconds to receive a controller reset from host. If the controller reset is not received within that time, firmware faults with fault code 0x070A. In some OS driver might take longer than 10 seconds to issue the controller reset.

Steps To Reproduce: Perform firmware downgrade in OS where driver takes more than 10 seconds to issue the controller reset.

ID: DCSG00906577

Headline: Response to OOB command is not sent on Internal Dynamic Memory Allocation failure

Description Of Change: Modified FW to return failure response to host on internal dynamic memory allocation failure.

Issue Description: On Internal Dynamic Memory Allocation failure while processing an OOB command, FW is not sending out a failure response to the user and as a result the command is timing out

Steps To Reproduce: Execute OOB commands with huge response length configured in the command request

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ID: DCSG00915992

Headline: Data length from host to DA-SEP device not checked if it is more than buffer length in firmware

Description Of Change: While transferring data from host to controller for processing a command sent to DA-SEP device, limit the data length based on size of buffer allocated by firmware.

Issue Description: Before sending the command to DA-SEP device firmware needs to transfer the data from host to a local buffer where I2C command is formed. There is no check to see if the data length in host command is more than the allocated buffer length so it might cause buffer overflow.

Steps To Reproduce: Not applicable.

ID: DCSG00918045 (Port Of Defect DCSG00916381)

Headline: Controller Faults when connected to DA SEP Backplane

Description Of Change: Fixed the PL FW to make sure the DA SEP Initialize function is invoked before vSES initialize function.

Issue Description: PL FW code flow has a known restriction where in vSES initialize function should always invoked only after invoking DA SEP Initialize function. As part of PL FW code clean up, this code flow was broken and hence the controller faulted when connected to a DA SEP backplane with vSES enabled in NVData.

Steps To Reproduce: 1. Flash Phase 17 or beyond code onto the controller (Note: vSES should be enabled in NVData)
2. Connect the controller to a DA SEP Backplane

Enhancements Implemented (3):

ID: DCSG00366048

Headline: SPDMLIB: Support SPDM Challenge command request for hash of all supported measurements

Description Of Change: Added support for computing hash of all supported measurements via Param2 field of the SPDM Challenge command.

In SPDM Lib, we would need to check for that request and compute:
hash(Concatenation(Measurement 1, Measurement 2, ..., Measurement N)) of all supported measurements.

Since Param2 field of the Challenge command can have other value, so the code has to check for other value and honors or fails the request:
0x0 = No Measurement Summary Hash,
0x1 = TCB Component Measurement Hash,
0xFF = All measurements Hash.
All other values reserved - reject SPDM Challenge command if BMC set this value in Param2.

Note:
For Aero we don't plan to support 0x1 = TCB Component Measurement Hash, so if BMC requests for this, SPDM Lib would return the hash size of all 0s. Starting in Avenger, we will support TCB.

ID: DCSG00383538

Headline: Summary of changes

Description Of Change: LIBMBEDTLS compiles for Aero using C99 but not Avenger which uses CPP.
The changes consist mostly of:

1.) Casts to set the variable type correctly for various assignments and function calls.
2.) Dealing with unused variables/parameters in a benign way.

ID: DCSG00813882

Headline: MBEDTLS LIB: Add license files to source tree

Description Of Change: Add license files to MBEDTLS LIB source tree: apache-2.0.txt and LICENSE.

ReleaseOrder ID: ***DCSG00904858*** Open In CQWeb
Headline: ***Alpha Release: CtrlFw_Ph_19.0 - 18.250.03.00 Firmware***
Release Version: ***18.250.03.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_19.0***
UCM Stream: ***CtrlFw_Ph_19.0_Rel***
Release Type: ***Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_19.0-2021-02-11-18.250.03.00_REL_1613060415@\SAS35***
Release Date: ***2021-02-11 16:19:42.000000***
Date Generated: ***Apr 26, 2021***

Defects Fixed (2):

ID: DCSG00839445
Headline: pl: backend PCIe: PCIe error handler fails to issue task management with cascading errors
Description Of Change: Fixed a PCIe error handler and PCIe task management interaction bug that caused the PCIe error handler level to be left in a non-idle state after sending a TM to an uninitialized device.
Issue Description: If a backend PCIe device isn't initialized and certain PCIe errors are detected on the link to which that device is connected, the PCIe error handler will fail to send task management requests to the device if subsequent PCIe errors occur.
Steps To Reproduce: Run a test that induces an error which results either in the root port halting inbound traffic or a link down during NVMe initialization. Then, induce additional errors of similar type.

ID: DCSG00831920 (Port Of Defect DCSG00654439)
Headline: (SATA Only) IO Timeouts seen while running Unmap, SATA Passthrough and Read/Write IOs to a SATA drive
Description Of Change: When NCQ Encapsulation for SCSI Unmap command is active and a non NCQ command is received, do not send a notification for hardware to pend all new fast path IOs. This will allow SCSI Unmap command to complete and not block other non NCQ IOs.
Issue Description: If a SATA drive supports Send/Receive FPDMA Queued command, a SCSI Unmap command is translated using NCQ encapsulation with Data Set Management as subcommand of Send FPDMA Queued command. Firmware sets a flag when NCQ encapsulation is active, so that any non NCQ command received is pended while the flag is set.
However when a non NCQ command is received, a notification is sent to the hardware so any new fast path command gets pended. This results in a deadlock situation as both NCQ and non NCQ commands are not able to progress resulting in timeouts.
Steps To Reproduce: To a SATA drive that supports Send/Receive FPDMA Queued command, send a SCSI Unmap command such that it results in sending multiple Send FPDMA Queued commands. While this is in progress send some non Read/Write IOs or SATA Passthrough commands.

Enhancements Implemented (2):

ID: DCSG00833193
Headline: SATL : ATA Passthruough command handling when Datalength in MPI < data requested to drive
Description Of Change: For ATA Passthrough command, the data transferred to host is calculated as minimum of Datalenght in MPI request and the data requested to drive.

ID: DCSG00903186 (Port Of EnhancementRequest DCSG00777328)
Headline: SEKM feature enhancements to handle error scenarios
Description Of Change: 1. Added code changes to abort an outstanding Send Host Message command if the MCTP interface is reinitialized by the host BMC.
2. Modified existing FW code to associate every Host Message Event with a unique Tag instead of using the Sequence Number sent as part of the Send Host Message command. This will ensure that if host BMC sends consecutive Send Host Message commands with the same sequence number, FW does not send response to BMC in case the Host Message Event Acknowledgement to the first Send Host Message command is received even though it has been aborted.

ReleaseOrder ID: ***DCSG00831518*** Open In CQWeb
Headline: ***Pre-Alpha Release: CtrlFw_Ph_19.0 - 18.250.02.00 Firmware***
Release Version: ***18.250.02.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_19.0***
UCM Stream: ***CtrlFw_Ph_19.0_Rel***
Release Type: ***Pre-Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_19.0-2021-01-28-18.250.02.00_REL_1611861279@\SAS35***
Release Date: ***2021-01-28 19:14:00.000000***
Date Generated: ***Apr 26, 2021***

Defects Fixed (5):

ID: DCSG00063448
Headline: pl: NVMe: Format Unit FMTDATA bit should be ignored
Description Of Change: Disregard the FMTDATA bit when processing a Format Unit command to an NVMe device.
Issue Description: Since the items contained within the Format Unit parameter list are currently unsupported, PL should ignore the parameter list data and the FMTDATA bit. Instead, the Format Unit command is rejected if the FMTDATA bit is set to 0.
Steps To Reproduce: Issue a Format Unit command to an NVMe device with the FMTDATA bit set to 0.

ID: DCSG00810786
Headline: SPDM lib compile error for Ventura build
Description Of Change: Fixed SPDM lib compile out error for Ventura build
Issue Description: SPMD definition included for Ventura
Steps To Reproduce: make all

ID: DCSG00830822 (Port Of Defect DCSG00430198)
Headline: [Aero][PLDM] PLDM Timer restart failing
Description Of Change: PLDM timer restart need to stop the timer, reset the time and then start the timer back again.
Issue is only observed with restart timer.
Issue Description: Once a timeout occurs in PLDM transfer ready state machine state machine it should return to idle state.
PLDM timer callback does not get called on timer expiry.
PLDM timer as part of restart stop and start the timer.
Steps To Reproduce: 1) Initiate the PLDM fw download via BMC emulator scripts.
2) One the FW download SM reaches transfer ready state.
3) Force the FW download to timeout.
4) Observe that PLDM fw download SM will not return back to idle state

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ID: DCSG00831123 (Port Of Defect DCSG00555977)
Headline: [Aero][OOB] Firmware download in loop from OOB in PCIe mode fails
Description Of Change: Clear the response from the queue once the response is transmitted.
Issue Description: When FW download in loop and some Asyn requests generated by FW some time response to a FW download request is not sent because of memory shortage in response queue. Responses of few commands from the queues are not released properly.
Steps To Reproduce: 1) Download the FW via out of band in loop.
2) Observe that FW download fails after 10 cycles.

ID: DCSG00707457 (Port Of Defect DCSG00653774)
Headline: HBA hangs on boot with failed UBM backplane in a multi-UBM backplane topology
Description Of Change: Updated PL to set No BP Mgmt. present on the connector UBM discovery failed and skip the connector modules where no UBM is detected when reading the UBM DFC SES status for VSES status diag page updates.
Issue Description: The HBA may hang during boot when one of the UBM backplane discovery fails in a multi-UBM backplane server topology. When UBM backplane discovery fails, the PL transitions the connector to backplane discovery complete state but flags UBM was detected. Since the PL flags UBM was detected on the connector, the VSES tries to read DFC SES status during SES diag page status updates and gets stuck in the state as the connector is in incorrect state to proceed with UBM DFC status read. This holds up the SES request completion back to RAID stack causing the boot up hang.
Steps To Reproduce: NA

Enhancements Implemented (12):

ID: DCSG00008204
Headline: PL : Remove obsolete workarounds
Description Of Change: Removed dead code related to workarounds that are already disabled across all products.

ID: DCSG00258258
Headline: Blackduck: Remove non UTF-8 encoding characters from source files
Description Of Change: Blackduck reported non UTF-8 encoded characters in source files.
Most of the characters are in header comment block of source files.
Replace such characters with their ASCII equivalents.

ID: DCSG00293141
Headline: MPI 2.6: Header file changes associated with revision 2.6.11
Description Of Change: Made all header changes associated with new proposals and editing updates for the 2.6.11 revision of MPI.

ID: DCSG00323525
Headline: BST: Bring up new Aero activity BST server at BLR
Description Of Change: Added support for running Aero activity BST on Linux Server

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ID: DCSG00351950
Headline: Update 9500-16i, 8i channel XMLs to support new VPP backplane management device address.
Description Of Change: Added support for new Gen-4 VPP backplane management device (I2C address 0x4C) to 9500-16i and 9500-8i channel boards xml.

ID: DCSG00408836
Headline: Integrate MPI 2.6.11 headers
Description Of Change: A new version of the MPI specification and headers has been released.
The headers for version 2.6.11 need to be integrated into Ventura/Aero releases.

ID: DCSG00481628
Headline: CFGI: Integrate MPI 2.6.11 headers with CFGI Lib.
Description Of Change: Latest MPI headers have a small change that affects CFGI.

ID: DCSG00707071
Headline: SPDM feature compile out from FW code
Description Of Change: Fixed compilation errors during SPDM feature code compiled out from the code base by disabling SPDM macro.

ID: DCSG00757333
Headline: pl: backend PCIe: target link speed diag command
Description Of Change: Added the "pl pci tls" diag console command to direct a PCIe endpoint or bridge to a certain target link speed for debug.

ID: DCSG00777312 (Port Of EnhancementRequest DCSG00433132)
Headline: SEKM Support for IT controllers
Description Of Change: 1. Implemented a new IOCParameter EKM_HELPER_PARAM (0x82) which will be used with GET_IOC_PARAMETER & SET_IOC_PARAMETER MPI IO Unit control request operation.
2. Implemented new IO Unit Control operation GET_IOC_PARAMETER (0x20)
3. Enabled user to be able to execute Send Host Message MPI command in OOB path. On receiving this command, FW will send Host Message Event to the OS driver. Multiple outstanding Send Host Message command is not supported.
4. Implemented new Product Specific Extended Page Type 0xE1 Page 0 to support this feature.
5. FW will set the Drive Ownership to Host BMC i.e set Bit 31 EKM_HELPER_PARAM IOCParameter to 0b whenever a drive is Hot Inserted
6. FW handling when MPI Send Host Message command Times out and BMC aborts the command.

ID: DCSG00500775 (Port Of EnhancementRequest DCSG00447989)
Headline: [Aero][PLDM] Platform changes to accommodate latest PLDM baseline
Description Of Change: Change the order of PLDM library header file inclusions in platform to accommodate new PLDM baseline.

ID: DCSG00816022 (Port Of EnhancementRequest DCSG00549524)
Headline: SEKM: Prevent firmware Download of firmware that do not support SEKM when SEKM is enabled.
Description Of Change: Added a Product specific flags field in the component image header. Firmware compiled with SEKM feature support will set the bit 0 of this new Product Specific flags field.
When SEKM is enabled by writing the enable bit in EKM page 0 then any firmware download where incoming firmware image do not have the SEKM flag set in the Product Specific flags field of the firmware component header will be failed.

ReleaseOrder ID: ***DCSG00757816*** Open In CQWeb
Headline: ***Pre-Alpha Release: CtrlFw_Ph_19.0 - 18.250.01.00 Firmware***
Release Version: ***18.250.01.00***
UCM Project: ***CtrlFw***
Sub UCM Project: ***CtrlFw_Ph_19.0***
UCM Stream: ***CtrlFw_Ph_19.0_Rel***
Release Type: ***Pre-Alpha***
State: ***Released***
Release Baseline: ***CtrlFw_Ph_19.0-2021-01-12-18.250.01.00_REL_1610449422@\SAS35***
Release Date: ***2021-01-12 11:02:55.000000***
Date Generated: ***Apr 26, 2021***

Defects Fixed (5):

ID: DCSG00501518
Headline: PL NVMe : IOs fail with SGL length shorter than the transfer legth
Description Of Change: Before starting read/write commands clear the context memory.
Issue Description: Stale flag data in the context memory leads to setting invalid length during SGL translation for IOs.
Steps To Reproduce: 1. Configuration consits of 2 Atlas switches
2. Run I/O to EPD on Atlas SW#1.
3. Run APC power cycle script (every couple minutes) on Atlas SW#2 to remove and add EPD drives

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ID: DCSG00552897
Headline: [Aero][UBM] Enhance the link configuration to handle the link speeds for SAS/SATA drives behind UBM.
Description Of Change: Configure the link speeds based on the speed reported by UBM for SAS/SATA drives behind UBM.
Issue Description: Nvdata changes made by applications gets more precedence to UBM reported link speeds.
Steps To Reproduce: 1) Connect a Ventura HBA to UBM which supports SAS/SATA drives.
2) Observe the link speeds of SAS/ SATA drives.
3) Now try to change the link speeds of SAS/SATA drives.
4) Observe that link speed configured by User gets more priority that the UBM reported link speed.

ID: DCSG00734511 (Port Of Defect DCSG00654031)
Headline: pl: SAS IO Unit Page 1 Write Current may not cause phy to be enabled
Description Of Change: Fixed a bug in the SAS IO Unit Page 1 Write Current handler that caused the protocol mode of a SAS/SATA phy to not be changed when the device side PCIe feature is disabled and the enable/disable state of the phy is modified in the page.

Note that this issue was introduced in PL phase 16.
Issue Description: If the device side PCIe feature is disabled and a SAS/SATA phy is disabled in SAS IO Unit Page 1 at port enable time, the protocol mode change that must occur to enable the phy is suppressed when Write Current of SAS IO Unit Page 1 is issued to enable the phy following port enable. This causes the phy to remain disabled.
Steps To Reproduce: Configure one or more phys as disabled in SAS IO Unit Page 1 NVDATA; that is, with the PhyData.PhyFlags.DisablePHY flag set to 1. Bring up firmware. Issue a Write Current to SAS IO Unit Page 1 with the DisablePHY flag set to 0.

ID: DCSG00757561 (Port Of Defect DCSG00654062)

Headline: Some drives and enclosures not added to Windows OS when SAS/SATA devices are reduced in NVDATA.

Description Of Change: Set the MaxTarget field of IOC Facts reply with (number of enclosure) * (number of phys per enclosure).

Issue Description: Windows driver uses MaxTarget field in IOC Facts reply to reserve total drive slots at SOD. Whenever there is a enclosure add, driver check if sufficient entries are available by using the max slot count. If entries are not available it will not add the enclosure and device under it to OS.

Since NumberOfTargets accounts only for SAS/SATA devices it might be insufficient for total number of possible slots.

Steps To Reproduce: Flash controller with FW where number of SAS/SATA devices are reduced to 32 in NVDATA. Attach a UBM backplane, a PCIe switch and an external enclosire to the controller. The enclosure and drives in it are not discovered in Windows OS.

ID: DCSG00708188 (Port Of Defect DCSG00708175)

Headline: [Aero] Phase 18 build error fix

Description Of Change: Proper handling of unused variable .

Issue Description: N/A

Steps To Reproduce: N/A

Enhancements Implemented (4):

ID: DCSG00122084

Headline: Enable collection of PCIe Link event "RECEIVED_NAK_DLLP" (EventCode=0x08) by default

Description Of Change: Updated PCIe Link Page-3 data to count the event "MPI26_PCIELINK3_EVTCODE_RECEIVED_NAK_DLLP" (EventCode=0x08) by default.
This event is added as a Saturating-Counter.

ID: DCSG00500552

Headline: PL SATL : Update the WRITE SAME command to account for Zoned Block Devices

Description Of Change: If write same is translated to SCT write same and the the ATA device is an ATA zoned device, then the ATA ZAC OPTIONS field is set to 8002h, otherwise the ATA ZAC OPTIONS field set to 0000h

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ID: DCSG00500554

Headline: Support downloading of the Host-based Trace Buffer (HTB) via MCTP OOB Interface on Ventura/Aero IOC/HBA (Part A)

Description Of Change: A new MCTP Command "TRACE_BUFF_OP" (Code=0x0E) added to allow downloading the Host-Trace-Buffer (HTB) data OOB to ScrutinyLib/BMC.
1. This command is disabled by default for Part-A.
2. The Trace-buffer-Operation command supports "Query" and "Read" Operations
   i. "Query" operation will return the current status of HTB buffer
   ii. "Read" operation will return the content of the HTB data segment requested (if allowed)

ID: DCSG00507210 (Port Of EnhancementRequest DCSG00500296)

Headline: [SPDM] Blocking slots 1-7 from configuring SPDM certificates

Description Of Change: As per OEM request blocking the certificate slots 1 to 7. Only slot 0 should be in use.
If the users attempt to send a command to program certificate from slot 1 - 7, FW will reject this command with invalid parameter status.
