ReleaseOrder ID:	*SCGCQ01564879*
Headline:	*Ventura IT: SASFW_Ventura_Phase_6.0 - 06.00.00.00*
Release Version:	*06.00.00.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Phase_6.0_Rel*
Release Type:	*GCA*
State:	*Deployed*
Release Baseline:	*SASFW_Ventura_Phase_6.0-2018-01-16-06.00.00.00_REL_1516135020@ \SAS_CTRL_FW*
Release Date:	*17-JAN-18*
Date Generated:	*Feb 16, 2018*

Release History

- **SCGCQ01558368 - Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.12.0**
- **SCGCQ01545189 - Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.11.0**
- **SCGCQ01530609 - Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.10.0**
- **SCGCQ01524136 - Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.09.0**
- **SCGCQ01520688 - Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.08.0**
- **SCGCQ01514304 - Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.07.0**
- **SCGCQ01507026 - Ventura IT: SASFW_Ventura - 05.250.05.00 Firmware**
- **SCGCQ01491728 - Ventura IT: SASFW_Ventura - 05.250.04.00 Firmware**
- **SCGCQ01487015 - Ventura IT: SASFW_Ventura - 05.250.03.00 Firmware**
- **SCGCQ01484480 - Ventura IT: SASFW_Ventura - 05.250.02.00 Firmware**
- **SCGCQ01470796 - Ventura IT: SASFW_Ventura - 05.250.01.00 Firmware**
- **SCGCQ01458609 - Ventura IT: SASFW_Ventura - 05.250.00.00 Firmware**

ReleaseOrder ID:	*SCGCQ01558368* Open In CQWeb
Headline:	*Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.12.0*
Release Version:	*05.250.12.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Phase_6.0_Rel*
Release Type:	*ReleaseCandidate*
State:	*Superseded*
Release Baseline:	*SASFW_Ventura_Phase_6.0-2018-01-10-05.250.12.00_REL_1515628676@ \SAS_CTRL_FW*
Release Date:	*12-JAN-18*
Date Generated:	*Feb 16, 2018*

Defects Fixed (2):

ID:	SCGCQ01556426 (Port Of Defect SCGCQ01522343)
Headline:	pl: backend PCIe: switch attached discovery takes too long
Description Of Change:	Modify the scheduling of switch attached discovery so that, in usual cases, it runs for additional time before yielding to other tasks.
Issue Description:	When a discovery run involving a PCIe switch occurs, it is likely that several PL timer ticks will elapse between the start and completion of the discovery run. This can cause other PL subsystems that are waiting on advancement of the discovery session, such as task management, to time out.
Steps To Reproduce:	Repeatedly issue target reset (hot reset) to switch attached NVMe devices while running heavy IO to them.

ID:	SCGCQ01556893 (Port Of Defect SCGCQ01540226)
Headline:	pl: backend PCIe: link workaround not sufficiently coordinated with SAS link establishment
Description Of Change:	Completely disable the offending workaround when a SAS or SATA link is established. Re-enable it after the SAS or SATA link goes down.
Issue Description:	A workaround for a PCIe link issue remains partially enabled when a SAS or SATA link comes up, and, if the workaround happened to be disabled, it is not re-enabled when the SAS/SATA link goes down.
Steps To Reproduce:	Code inspection.

ReleaseOrder ID:	*SCGCQ01545189* Open In CQWeb
Headline:	*Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.11.0*
Release Version:	*05.250.11.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Phase_6.0_Rel*
Release Type:	*Beta*
State:	*Superseded*
Release Baseline:	*SASFW_Ventura_Phase_6.0-2017-12-21-05.250.11.00_REL_1513897394@ \SAS_CTRL_FW*
Release Date:	*08-JAN-18*
Date Generated:	*Feb 16, 2018*

Defects Fixed (3):

ID:	SCGCQ01529512 (Port Of Defect SCGCQ01509770)
Headline:	PL: Fault 0x5862 seen when host buffer size is smaller than allocation length in CDB
Description Of Change:	Added check inside plSataHandleScsiGetPhysicalElementStatus () for making sure we always have enough host buffer before setting the sata hardware engine for automated transfer of data. If host buffer is too small, terminate the command with pl loginfo.
Issue Description:	For SATA drives which support depopulation feature, when issued with get physical element status command with receive buffer size from host set to value smaller than allocation length in CBD for command, fault 0x5862 can be observed. This is due to RX hardware reaching end of SGL address but still has data to transfer causing interrupt.
Steps To Reproduce:	Using sg_raw, send get physical element status command CDB with allocation size greater than host buffer size set with -r option.

ID: SCGCQ01533267 (Port Of Defect SCGCQ01530402)

Headline: pl: NVMe: EC0D fault

Description Of Change: Issue an internal target reset to an NVMe device if PCIe reconfiguration is found to be necessary while NVMe init is running.

Issue Description: If PCIe reconfiguration occurs for an NVMe device while NVMe initialization is running, an EC0D fault may occur.

Steps To Reproduce: Perform link glitch testing with an NVMe device that malfunctions when such testing is performed.

ID: SCGCQ01539840 (Port Of Defect SCGCQ01531770)

Headline: PL Fault 0000ecdd LR 01403837 during initial discovery

Description Of Change: Modified management of protocol cycling to disable PCI link management for a link once SAS or SATA devices are detected on a phy within the link.

Issue Description: During start of day discovery, system faults with 0xECDD when setup is configured for tri-mode serdes and SAS/SATA drives are attached.

Steps To Reproduce: Attached SAS/SATA devices to controller configured for tri-mode support and initialize.

ReleaseOrder ID:	*SCGCQ01530609* Open In CQWeb
Headline:	*Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.10.0*
Release Version:	*05.250.10.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Phase_6.0_Rel*
Release Type:	*Beta*
State:	*Superseded*
Release Baseline:	*SASFW_Ventura_Phase_6.0-2017-12-12-05.250.10.00_REL_1513118224@ \SAS_CTRL_FW*
Release Date:	*13-DEC-17*
Date Generated:	*Feb 16, 2018*

Defects Fixed (6):

ID: SCGCQ01524353 (Port Of Defect SCGCQ01516277)

Headline: (SATA Only) LBPRZ bit in VPD page 0xB2 is never set for SATA devices

Description Of Change: Added setting LBPRZ in logical block provisioning VPD page (pagecode 0xB2) when RZAT bit is set in identify data.

Issue Description: As per SAT spec LBPRZ bit in logical block provisioning page should be set for SATA devices when RZAT bit is set its identify data.

Steps To Reproduce: Attach a SATA SSD drive with support for data set management commands and RZAT bit set in its identify data. Send inquiry command for vpd page 0xB2 to the drive and notice that LBPRZ bit is not set in the response.

ID: SCGCQ01524638 (Port Of Defect SCGCQ01275335)

Headline: (SATA Only) Security Protocol In command complete without data transfer for allocation length not a multiple of 512

Description Of Change: Since SATA drive transfer data in multiples of 512 byte sectors, fail any Security Protocol command with Security Protocol set to value other than SAT Specific where allocation length is not a multiple of 512 with Check Condition and sense key set to illegal request and additional sense code set to invalid field in CDB.

Issue Description: For Security Protocol In command when Security Protocol is set to a value other than SAT Specific (0xEF) the data read from drive is in multiple of 512 byte sectors. While sending the translated ATA command to the drive allocation length is used as the data length and the data transfer to host is automated. Now if allocation length is not in multiple of 512 it results in over run error reported by hardware which results in command and data transfer getting aborted.

Steps To Reproduce: Send a Security Protocol In command with Security Protocol set to 0 and Allocation Length set to value not a multiple of 512. Observe the command complete without getting any data back.

ID: SCGCQ01527219 (Port Of Defect SCGCQ01526236)

Headline: pl: NVMe: PCIe reconfiguration may occur during NVMe controller reset

Description Of Change: Fixed an issue that caused discovery to improperly conclude that an NVMe device undergoing controller reset had not been configured.

Issue Description: When an NVMe task management that issues NVMe controller reset is outstanding to an NVMe device, if PCIe discovery happens to run, PCIe configuration may be unexpectedly performed for the device.

Steps To Reproduce: Issue a task management type that generates NVMe controller reset to an NVMe device. Then, cause PCIe discovery to run on the root port to which the device is attached.

ID: SCGCQ01529383 (Port Of Defect SCGCQ01516968)

Headline: pl: backend PCIe: non-NVMe endpoint not cleaned up on removal

Description Of Change: Do not generate PL structures for an unsupported PCIe endpoint. Unsupported PCIe endpoints are now ignored by PL.

Issue Description: If a non-NVMe device is attached to a device side PCIe port, the PL structures associated with the device aren't cleaned up when the device is removed.

Steps To Reproduce: Connect a non-NVMe device to Ventura and then remove it.

ID: SCGCQ01530305 (Port Of Defect SCGCQ01450475)

Headline: Get VDM Support command does not have VendorID and VendorAddInfo fields properly populated

Description Of Change: VendorId is populated correctly now.

Issue Description: VendorId is not populated correctly.

Steps To Reproduce: 1) Update the controller with Ventura Main.
2) From BMC try pulling VendorDefined Message Support.
3) observe that vedorId is not correct.

ID: SCGCQ01530310 (Port Of Defect SCGCQ01494018)

Headline: Controller is not detecting in the storelib, after changing the mode from "set mode oob" command

Description Of Change: changing the code in handling RESPOND_SLAVE flag only when binding is set to PCIE.

Issue Description: ManPage 19 NVDATA flags are changed to enable pcie mode, but I2C respond is slave mode flag are still retained.
Response to storelib is not handled properly when both I2C and PCIE flags are enabled.

Steps To Reproduce: 1. With the I2C and PCIe changes in NVDATA, flashed the controller fw on the 9400-16i card
2. Change the mode from I2C to PCIe using the command "set mode oob =pcie maxpayloadsize=1024 maxpacketseize=0080"
3. Powercycle and restart the server.
4. Observe in the storelib, Controller is not detected.

ReleaseOrder ID:	*SCGCQ01524136* Open In CQWeb
Headline:	*Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.09.0*
Release Version:	*05.250.09.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Phase_6.0_Rel*
Release Type:	*Beta*
State:	*Superseded*
Release Baseline:	*SASFW_Ventura_Phase_6.0-2017-12-05-05.250.09.00_REL_1512526690@ \SAS_CTRL_FW*
Release Date:	*07-DEC-17*
Date Generated:	*Feb 16, 2018*

Defects Fixed (3):

ID: SCGCQ01522342
Headline: pl: backend PCIe: 4311 fault with NVMe enabled (part 2)
Description Of Change: Perform additional checks to ensure that a sub-block of the phy hardware has gone idle before proceeding with phy hardware cleanup.
Issue Description: After a device side PCIe hot reset or link down, a 4311 fault may occur.
Steps To Reproduce: Attach an NVMe device to the HBA and repeatedly disturb the link between the device and HBA.

ID: SCGCQ01522511 (Port Of Defect SCGCQ01487423)
Headline: pl: NVMe: rapid device removal/add with a specific vendor backplane
Description Of Change: When a device presence poll occurs with the specific vendor backplane, the backplane reports that the PERST# signal is asserted, and PL believes that the signal should be deasserted, PL will deassert PERST# even if the device presence state has not changed.
Issue Description: If an NVMe device is disconnected from a specific vendor backplane and is then reconnected within the configured device presence polling period, the device may be held in reset and consequently not link up.
Steps To Reproduce: Pull an NVMe device from the specific vendor backplane and then immediately reattach it.

ID: SCGCQ01523550 (Port Of Defect SCGCQ01523531)
Headline: pl: backend PCIe: 4311 fault with NVMe enabled (part 2)
Description Of Change: Perform additional checks to ensure that a sub-block of the phy hardware has gone idle before proceeding with phy hardware cleanup.
Issue Description: After a device side PCIe hot reset or link down, a 4311 fault may occur.
Steps To Reproduce: Attach an NVMe device to the HBA and repeatedly disturb the link between the device and HBA.

ReleaseOrder ID:	**SCGCQ01520688** Open In CQWeb
Headline:	**Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.08.0**
Release Version:	**05.250.08.00**
UCM Project:	**SAS3.5FW_MASTER_DEV**
Sub UCM Project:	**SASFW_Ventura_Phase_6.0**
UCM Stream:	**SASFW_Ventura_Phase_6.0_Rel**
Release Type:	**Beta**
State:	**Superseded**
Release Baseline:	**SASFW_Ventura_Phase_6.0-2017-11-30-05.250.08.00_REL_1512087652@ \SAS_CTRL_FW**
Release Date:	**04-DEC-17**
Date Generated:	**Feb 16, 2018**

Defects Fixed (4):

ID: SCGCQ01519729 (Port Of Defect SCGCQ01514880)
Headline: Ventura hardware does not like the IOP enable method used here.
Description Of Change: Use a different sequence to enable the IOP interrupt for Ventura HW.
Issue Description: Controller is not detecting in storelib after flashing the latest firmware (5.250.7.0) on OEM platform.
Steps To Reproduce: Use storelib or BMC emulator to connect to Ventura platform.

ID: SCGCQ01519732
Headline: Ventura: 4311 fault with NVMe enabled
Description Of Change: Ensure that a sub-block of the phy hardware has gone idle before proceeding with phy hardware cleanup.
Issue Description: After a device side PCIe hot reset or link down, a 4311 fault may occur.
Steps To Reproduce: Attach NVMe devices to a Ventura HBA.

ID: SCGCQ01519802 (Port Of Defect SCGCQ01518343)
Headline: pl: backend PCIe: workaround timer may trigger after too short of an interval
Description Of Change: Validate the workaround timer elapsed time with the global free running timer before running the workaround.
Issue Description: If global timer catchup ticks occur, a timer associated with the backend PCIe polarity inversion stuck workaround may run for less than the expected time before triggering, causing the link to be unexpectedly hot reset.
Steps To Reproduce: N/A

ID: SCGCQ01520574 (Port Of Defect SCGCQ01514521)
Headline: pl: backend PCIe: 4311 fault with NVMe enabled
Description Of Change: Ensure that a sub-block of the phy hardware has gone idle before proceeding with phy hardware cleanup.
Issue Description: After a device side PCIe hot reset or link down, a 4311 fault may occur. This issue was introduced with phase 6 firmware.
Steps To Reproduce: Attach NVMe devices to a Ventura HBA.

ReleaseOrder ID:	**SCGCQ01514304** Open In CQWeb
Headline:	**Ventura IT: SASFW_Ventura_Phase_6.0 - 05.250.07.0**
Release Version:	**05.250.07.00**
UCM Project:	**SAS3.5FW_MASTER_DEV**
Sub UCM Project:	**SASFW_Ventura_Phase_6.0**
UCM Stream:	**SASFW_Ventura_Phase_6.0_Rel**
Release Type:	**Beta**
State:	**Superseded**
Release Baseline:	**SASFW_Ventura_Phase_6.0-2017-11-22-05.250.07.00_REL_1511419200@ \SAS_CTRL_FW**
Release Date:	**24-NOV-17**
Date Generated:	**Feb 16, 2018**

Defects Fixed (1):

ID: SCGCQ01514262 (Port Of Defect SCGCQ00856085)
Headline: Fault State (0x265d) is Observed While Connecting an Enclosure with Fully Populated SATA Drives
Description Of Change: To fix the issue, in the Passthrough callback functions(Complete Drive Diagnosis, Complete DMA, Passthrough DMA), the freeing of the temporary message frame should be done only in cases where the SATA Passthrough Complete function will not be called for the same request.
Issue Description: - In case of SATA Passthrough Command request, a temporary message frame is created by PL, which saves the original message frame from IOP.
- Later in the SATA Passthrough Complete function for the request, the contents of the temporary frame is copied back to the original message frame and then the temporary frame is freed.
- Inside certain Passthrough callback functions (Complete Drive Diagnosis, Complete DMA, Passthrough DMA), the temporary message frame is getting freed before the SATA Passthrough Complete function is called.
- These functions get invoked when the SATA Drive is detected by the controller.
- So when the SATA Passthrough Complete function is called afterwards for the same request, when it tries to copy the contents of the temporary frame, a FAULT is generated because the frame has already been freed.
Steps To Reproduce: Flash the SAS3 controller with latest firmware and connect an enclosure with fully populated SATA drive to controller. Firmware fault 0x265d is hit and can be observed in driver logs.

ReleaseOrder ID:	***SCGCQ01507026*** <u>Open In CQWeb</u>
Headline:	***Ventura IT: SASFW_Ventura - 05.250.05.00 Firmware***
Release Version:	***05.250.05.00***
UCM Project:	***SAS3.5FW_MASTER_DEV***
Sub UCM Project:	***SASFW_Ventura_Phase_6.0***
UCM Stream:	***SASFW_Ventura_Rel***
Release Type:	***Alpha***
State:	***Superseded***
Release Baseline:	***SASFW_Ventura-2017-11-10-05.250.05.00_REL_1510357587@ \SAS_CTRL_FW***
Release Date:	***13-NOV-17***
Date Generated:	***Feb 16, 2018***

Defects Fixed (15):

ID: SCGCQ01451278
Headline: pl: backend PCIe: link may fail to come up after link break
Description Of Change: Worked around an issue that causes backend PCIe lane polarity inversion to become stuck on.
Issue Description: If a backend PCIe link is broken and then reconnected, the link may fail to come up until an adapter reset is performed.
Steps To Reproduce: Perform cable break testing with a variety of NVMe devices.

ID: SCGCQ01478170
Headline: Ventura vSES: Direct attached NVME drives are not getting associated with vSES in Microsoft Storage Spaces Direct.
Description Of Change: Program SAS address of the NVME drive in device id vpd page of the drive and additional elements status diagnostic page of vSES.
Issue Description: The SAS address of NVME device returned in device's device id vpd page (pagecode 0x83) should match with the SAS address field in one of the element of the additional elements status diagnostic page (pagecode 0xA) of enclosure for Microsoft S2D to associate a device with the enclosure. Firmware was not filling the SAS address of NVME devices in those pages.
Steps To Reproduce: Directly attach a NVME device to controller, "PhysicalLocation" Detail for NVMe drive does not provide slot information of the device in output of "Get-StorageFaultDomain" Command.

ID: SCGCQ01484382
Headline: pl: NVMe: improved fix for 6001 fault
Description Of Change: Refrain from issuing the NVMe commands that are issued during an Abort Task to the NVMe device if the targeted mid is found in an internal queue.
Issue Description: A more thorough fix for a recently fixed 6001 fault was identified during discussion about another issue related to task management.
Steps To Reproduce: Issue Abort Task task management requests to NVMe devices during IO.

ID: SCGCQ01485060
Headline: (SATA Only) Format of SATA SSD takes long time
Description Of Change: LBPWS (logical block provisioning with write same(16)) bit of logical block provisioning VPD page for SATA drive is set only when the drive supports ZERO EXT command.
Issue Description: If the drive reports LBPWS bit set in logical block provisioning page (pagecode 0xB2), then OS sends SCSI Write Same command with Unmap=1 to unmap the drive LBAs. The handling of SCSI Write Same with unmap=1 to SATA drives was changed to use ATA ZERO EXT command instead of DATA Set Management Trim commands but the LBPWS bit was still set even if drive does not support ZERO EXT command.
Steps To Reproduce: 1. Attach a SATA SSD disk to the controller.
2. Use Linux fdisk tool to create one partition using full size of the disk.
3. Use Linux mkfs.ext4 command to format the partition.

Format takes long time to complete.

ID: SCGCQ01485441
Headline: Ventura/Marlin: Firmware Download does not protect user from downgrading to firmware that does not support Winbond
Description Of Change: Add checks in the firmware that will send a failure if incompatible firmware is downloaded.
Issue Description: If the user downloads firmware that will not work with the new Windbond 256Mbit part, future firmware downloads will fail
Steps To Reproduce: On a card with firmware that supports Winbond 256Mbit and has been programmed correctly, perform a firmware download of firmware that does not support that part

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ID: SCGCQ01487291
Headline: pl: NVMe: switch attached devices not detected under Windows
Description Of Change: Fixed an issue that caused Enclosure Device Status Change events to not be generated for switches following a message unit reset.

Fixed an issue that caused port enable to complete before PCIe Topology Change List events were generated following a message unit reset.
Issue Description: If the BIOS loads and switch attached NVMe devices are discovered, and Windows is then booted, the switch attached devices will not show up in the OS.
Steps To Reproduce: Load the ROM BIOS onto a Ventura board. Connect switch attached NVMe devices and boot the host system into Windows.

ID: SCGCQ01489030
Headline: Global HDD LED may not indicate IO activity for NVMe or SAS drives
Description Of Change: Changed FW to setup correct LED control MUX to select appropriate PHYs activity signal based on the device type discovered.
Issue Description: LED connected to global HDD activity header or using vendor specific connection on SAS3508/3408 based HBAs may not blink during IOs to NVMe HDD/SAS HDD. The FW enables LED control MUX by selecting the appropriate PHY activity signal based on the device type detected and this is setup incorrectly for 8-PHYs controller, not mapping the correct activity signal to the global activity LED to blink.
Steps To Reproduce: Connect a LED to global HDD activity header or using vendor specific connection on SAS3508/3408 based HBA, run IOs to NVMe HDD/SAS HDD and observe no LED activity.

ID: SCGCQ01496842
Headline: pl: SATA: port enable may time out on spinup failure
Description Of Change: Fixed a bug that caused the initial FIS wait retry counter to wrap prior to reaching the expected threshold.
Issue Description: If SATA spinup fails, PL is expected to retry it for an amount of time that is based on the spinup settings configured in NVDATA and then allow port enable to complete. There is however an issue that causes the number of retries to be effectively unlimited which may in turn cause port enable to time out.
Steps To Reproduce: N/A

ID: SCGCQ01497080
Headline: IOP MCTP: Changes missing from a previous code change
Description Of Change: Ported missing changes to the Intruder/Ventura stream.
Issue Description: During a code inspection, it was observed some changes that were ported from Invader to Intruder/Ventura were missing.
Steps To Reproduce: Not Applicable.

ID: SCGCQ01503262
Headline: Ventura FW may fault on single bit correctable ECC errors in IOA Local RAM
Description Of Change: Disabled error reporting for correctable single bit ECC errors in IOA local RAM.
Issue Description: Since HW corrects single bit ECC errors in IOA local RAM, the FW should not consider this an error and should not fault. There has not been a failure observed in the field.
Steps To Reproduce: N/A

ID: SCGCQ01504284
Headline: pl: backend PCIe: additional phy hardware cleanup on link down and hot reset
Description Of Change: Perform additional backend PCIe phy hardware cleanup on link down and hot reset.

Issue Description: Investigation has shown that additional cleanup of the backend PCIe phy hardware is required on link down and hot reset. Otherwise unexpected link failures may occur after link down or hot reset.

Steps To Reproduce: Perform link break and glitch testing with a specific vendor NVMe device.

ID: SCGCQ01504310

Headline: pl: backend PCIe: LTSSM state wait during hot reset

Description Of Change: Ensure that the L0 state has been reached before proceeding to issue hot reset.

Issue Description: When modifying link speed before performing a hot reset, it is expected for firmware to wait for hardware to report that it is in the L0 LTSSM state before continuing to issue the reset. This may not occur.

Steps To Reproduce: N/A

ID: SCGCQ01505392

Headline: Ventura: Slot LEDs on SGPIO based backplane may not blink

Description Of Change: Updated FW to configure the SGPIO HW with correct SClock frequency.

Issue Description: Recent changes to optimize the RMW operations of SGPIO HW initialization caused the SClock to be configured incorrectly so no data was sent out on the SGPIO stream to the backplane for slot LED control.

Steps To Reproduce: Connect 9400-16i HBA to SGPIO backplane with SAS/SATA drives and perform Locate operation to any of the slots using StoreCli utility. Observe the Amber LED not blinking.

ID: SCGCQ01468156 (Port Of Defect SCGCQ01180961)

Headline: Limit printing a SGL chain to only 15 elements.

Description Of Change: Revised the firmware so that the temporary buffer can't be overwritten.

Issue Description: If a SGL chain has more than 15 elements, it will not fit in a single frame buffer, and this can cause a core exception.

Steps To Reproduce: Can't be reproduced with current products.

ID: SCGCQ01505080 (Port Of Defect SCGCQ01498114)

Headline: PL SATL: SCSI Write Buffer Mode 7 Command Incorrectly Failed by Firmware

Description Of Change: Changed a validation check in SATL to follow what the SAT3 spec says and allow this case.

Issue Description: If a SATA drive reports its maximum and minimum supported number of firmware download blocks are both 0, PL SATL will fail any SCSI write buffer mode 7 command to that drive. Technically, this is incorrect, according to the SAT3 spec. Only if the maximum number of blocks is non-zero should it be checked against the number of blocks specified in the command.

Steps To Reproduce: Find a SATA drive that reports 0 for maximum and minimum supported number of firmware download blocks. Send a SCSI write buffer mode 7 command to that device handle. PL SATL will fail it with illegal request/invalid field in CDB.

Enhancements Implemented (1):

ID: SCGCQ01499168 (Port Of EnhancementRequest SCGCQ00878239)

Headline: Enhance SAS3 FW to pass PCIeCV PCIe Configuration Validation TD_1_28 Vital Product Data Capability Test

Description Of Change: New logic has been added during StartOfDay to look at Man Page 1 for valid VPD information. If all the VPD bytes are 0s, it will turn off VPD Capability.
So that the PCIE Capabilities List doesnt show an ID=0x3 (thats for VPD) and the PCI SIG test will pass.

ReleaseOrder ID:	*SCGCQ01491728*
Headline:	*Ventura IT: SASFW_Ventura - 05.250.04.00 Firmware*
Release Version:	*05.250.04.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Rel*
Release Type:	*Alpha*
State:	*Superseded*
Release Baseline:	*SASFW_Ventura-2017-10-27-05.250.04.00_REL_1509169904@ \SAS_CTRL_FW*
Release Date:	*30-OCT-17*
Date Generated:	*Feb 16, 2018*

Defects Fixed (7):

ID: SCGCQ01472941

Headline: Ventura VSES: Incorrect data in diagnostic page 0xA when drive is missing but not yet removed.

Description Of Change: Instead of reading device protocol information from phy structures read it from device data structure.

Issue Description: When the drive is missing but not yet removed from firmware as device missing delay is yet to expire the data in additional elements status diagnostic page (page code 0xA) might be incorrect. Firmware was reading some information from the phy data structures to fill the diagnostic page but when the device is removed those structures get cleared and data is no longer there.

Steps To Reproduce: 1. Attach a SAS/SATA drive directly to controller and read diagnostic page 0xA.
2. Remove the drive from controller and read the diagnostic page 0xA again before device is removed from firmware and host.
The data returned in diagnostic page step 1 and 2 does not match.

ID: SCGCQ01479409

Headline: SATL: Security Protocol Erase fails in SATL, but works well with ATA PT.

Description Of Change: Since the number of SATA INIT commands initiated from firmware is many(not just before Erase of this case), the new change will avoid SATA initialization for all the allowed commands when secure locked.
This change will avoid Initialization sequence between ErasePrepare and Erase, thus enabling Erase to work well.

Issue Description: Under SCSI Security Protocol(0xB5) ATA(0xEF) option - ErasePrepare(0xF3) and Erase(0xF4) are 2 commands to be run back to back.
As per present SATL design if drive is Secure Locked, the SATA initialization state is set to INIT_NEEDED forcing Initialization sequence before every command. This is to check if drive is unlocked and to make IOs fall through special IO handling path.
Between ErasePrepare(0xF3) and Erase(0xF4) there is a SATA_INIT sequence initiated by firmware as above, so the ErasePrepare context is lost in drives, thus Erase is aborted from drive.

Steps To Reproduce: 1.Send Identify command and verify that the drive is security enabled.
2.Send SECURITY PROTOCOL OUT command to LOCk the drive
3.send Erase unit command and command Fails

ID: SCGCQ01480646

Headline: pl: NVMe: task management timeout may occur

Description Of Change: When performing a PCIe hot reset to an NVMe device, wait up to ReportDeviceMissingDelay seconds for the device to link back up before considering the task management request to have timed out.

Issue Description: If a task management request is sent to an NVMe device that causes PCIe hot reset to be sent to the device, the task management request may unexpectedly time out.

Steps To Reproduce: Perform cable break testing with NVMe devices.

ID: SCGCQ01485059

Headline: pl: 265D fault on 'pl dbg' before port enable

Description Of Change: Prevent execution of some diag console commands if PL has not been initialized.

Issue Description: If the 'pl dbg' diag console command is issued before PL has been initialized, a 265D fault will occur.

Steps To Reproduce: Issue the 'pl dbg' diag console command before port enable has occurred.

ID: SCGCQ01489981

Headline: Code Unstable in Common_Main, Re definitions of Macro IOP_TIMED_CONDITION, consolidating them.

Description Of Change: Build Failure, Resolving code conflict.

Issue Description: Build Failure, Resolving code conflict.

Steps To Reproduce: Build Failure, Resolving code conflict.

ID: SCGCQ01455876 (Port Of Defect SCGCQ01385782)

Headline: MCTP I2C: I2C communication is lost between BMC and controller

Description Of Change: Added firmware code to enable and handle the Master Address NAK, Data NAK, and Slave IBML timeout interrupts.
Added firmware code to disable the slave receiving when about to transmit I2C Writes. And re-enable slave receiving when a transfer is done.
Changed the code to align the addresses of the data buffers used to transmit data.
Added stronger synchronization barriers before starting the transfer hardware.
Added detection for a certain BMC use-case where it is advantageous for the firmware to automatically Abort an existing command when a new command of the same Application Message Tag comes in.

Issue Description: The I2C communication is lost between the BMC and controller due to:
1. The transfer hardware with the I2C being used does not recognize some errors, and firmware does not handle either. Includes Master Address NAK, Data NAK, and broken I2C writes to the Slave.
2. FW not managing the transfer hardware using with the I2C in a highly serialized fashion, and with strong enough barriers before starting the transfer

Steps To Reproduce: With the firmware configured for true MCTP I2C (acts as Master and Slave on the bus) run many request over the bus.
Break the bus in various ways to cause the above issues.

ID: SCGCQ01488146 (Port Of Defect SCGCQ01410607)

Headline: BMC emulator on Ventura failed with Storlib discovery

Description Of Change: 1) pbam.h was modified to align with spec as part of SCGCQ00913173.
2) PBAM DCR Register offset got changed and broke the I2C DMA functionality.
3) corrected the DCR register offset.

Issue Description: 1) Controller is not detected on storelib with Phase4 and Phase5 GCA

Steps To Reproduce: 1) Flash the Controller with Ventura Phase4 or Phase5 GCA.
2) Try observing the controller information from storelib.
3) Controller is not detected on storelib.

Enhancements Implemented (1):

ID: SCGCQ01487366

Headline: pl: NVMe: add debug print to the NVMe encapsulated failure path

Description Of Change: Added a debug print to the NVMe encapsulated failure path.

ReleaseOrder ID:	*SCGCQ01487015* Open In CQWeb
Headline:	*Ventura IT: SASFW_Ventura - 05.250.03.00 Firmware*
Release Version:	*05.250.03.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Rel*
Release Type:	*Pre-Alpha*
State:	*Test_Complete*
Release Baseline:	*SASFW_Ventura-2017-10-25-05.250.03.00_REL_1508923562@ \SAS_CTRL_FW*
Release Date:	*27-OCT-17*
Date Generated:	*Feb 16, 2018*

Defects Fixed (3):

ID: SCGCQ01440764

Headline: Ventura B0: Fault 0x510B while doing reboot test along with IOs & TMs

Description Of Change: Task management requests which do not abort any IOs, have a slightly different firmware path. When the hardware starts the last IO for a device at the same time that a non-aborting Task management request is being processed, firmware may inadvertently reset a flag that hardware cleared. This causes the next IO to be enqueued improperly and is eventually detected as a corrupted queue. The change is for firmware to clear all the hardware flags if the control queue is empty.

Issue Description: When issuing all types of random Task Management requests and doing IOs, the controller faults with code 0x510b.

Steps To Reproduce: 1. Connect HBA & boot to os.
2. Connect drives & verify drives getting discovered.
3. Start a script to send random TM to random drive continuously.
4. Start read only IOs to all connected drives for 15 min.
       LinuxSmash -T /root/Desktop/IO/targets -iv 2 -dt 2 -tlimit 15 -nc INODE,DEVNO,SYSID,TIME,LBA,CRC,THREADID,PATTERN,HEADNTAIL
5. After 15 min reboot the server.
6. Repeat step 3-5.

Result: Fault 0x510B observed after ~3 Hrs.

ID: SCGCQ01480987

Headline: Ventura B0: Controller Reset causing OS hang and resets

Description Of Change: Switch PIM2 back to AXI mode after firmware upload completes. This will prevent firmware from wiping out the MSIx table on a subsequent soft reset.

Issue Description: Host MSIx table is getting incorrectly erased during a soft reset of the adapter since PIM2 got set to bit bucket mode during firmware upload process.

Steps To Reproduce: Perform a soft controller reset.

ID: SCGCQ01482937

Headline: MPI SEP request to Slots with invalid SES Page 0A element index may not complete

Description Of Change: Changed FW to fail SEP request if no element index is available with SES page 0Ah mapping is complete.

Issue Description: PL Enclosure management module creates a map of SES page 0Ah element index to device slot numbers on a MPI request and if the slot does not have a valid element index (eg. VSES slot), then page 0Ah is read again and this goes on, not completing the SEP request.

Steps To Reproduce: Send a MPI SEP request to VSES/SEP slot and observe the request not completing.

Enhancements Implemented (1):

ID: SCGCQ01479502 (Port Of EnhancementRequest SCGCQ01472512)

Headline: PL: Add Code to Correctly Determine Mid for Rx Context Non-automated Interrupts

Description Of Change: Added code in rx context non-automated handler function to correctly determine the mid, depending on protocol and frame type.

ReleaseOrder ID:	*SCGCQ01484480* Open In CQWeb
Headline:	*Ventura IT: SASFW_Ventura - 05.250.02.00 Firmware*
Release Version:	*05.250.02.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*

UCM Stream:	SASFW_Ventura_Rel
Release Type:	Pre-Alpha
State:	Superseded
Release Baseline:	SASFW_Ventura-2017-10-23-05.250.02.00_REL_1508800313@\SAS_CTRL_FW
Release Date:	25-OCT-17
Date Generated:	Feb 16, 2018

Defects Fixed (10):

ID: SCGCQ01405083
Headline: The Avoid Duplicate Mid feature does not activate properly for expander attached SATA devices
Description Of Change: Change which device info bits are used to determine expander attached SATA devices.
Issue Description: Target reset is not checkpointed or performed on expander attached SATA devices when they return after being missing.
Steps To Reproduce: Found by inspection, but can be tested by doing cable pull tests with expander attached SATA devices.

ID: SCGCQ01440481
Headline: SGPIO Clock driven Low on host PCIe reset assertion causing SGPIO target to latch on invalid data
Description Of Change: Modified FW to initialize the GPIO sideband Alternate data source CCR register to GPIO on PCIe/Chip reset and configure it later based on the backplane attached.
Issue Description: When GPIO Alternate source is selected as SGPIO, on a host PCIe reset the SGPIO clock signal may be driven low as the CCR registers retains the previous settings during reset. This may cause SGPIO target to treat the SClock transition as a valid clock and latch on to invalid data bit, indicating incorrect slot LED status.
Steps To Reproduce: Issue repeated PCIe resets while SIO data is transmitted and observe fault LED turned ON for a slot

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ID: SCGCQ01448752
Headline: Ventura: NVMe : Log Sense Command Executed for Information Exceptions Log Page has TSD field set to 0b
Description Of Change: Set the TSD field to set to 1b during Information Exceptions Log page translation.
Issue Description: As per NVMe SCSI translation document, the TSD field has to be set to 1b.
Steps To Reproduce: Issue Log sense command on a NVMe drive for retrieving the Information Exceptions Log page

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ID: SCGCQ01458388
Headline: (VSES) SES INQUIRY commands and storcli commands hang while getting adapter information
Description Of Change: Increase VSES command queue depth to match DA-SEP command queue depth and make sure VSES command complete code handles restarting pended MIDs for all corner cases to prevent pend Ios from being stuck forever.
Issue Description: PL firmware pends VSES commands in internal Pend Queue when it receives more than 1 VSES commands at a time. These pended commands never get started under certain conditions resulting in IOCTL timeouts at the host.
Steps To Reproduce: Issue streams of VSES commands from a host application.

ID: SCGCQ01464247
Headline: pl: NVMe: issues related to port enable completion
Description Of Change: Do not complete port enable unless all SAS and PCIe discovery sessions have completed.

Fixed an issue that caused the function to be called twice.

Ensure that both SAS and PCIe discovery have completed before configuring activity monitoring.
Issue Description: If one or more NVMe devices link up during port enable, port enable may complete before device discovery has completed.

A function involved with port enable completion is unexpectedly called twice when device initialization completes.

Activity monitoring may be configured before both SAS and PCIe discovery have completed.
Steps To Reproduce: Connect both SAS and NVMe devices to the HBA using OEM specific backplanes and bring up firmware.

ID: SCGCQ01472531
Headline: pl: NVMe: port enable may complete before devices link up
Description Of Change: Ensure that some time elapses between the completion of backplane initialization and discovery of NVMe devices.
Issue Description: If an OEM specific NVMe backplane is attached to the HBA, port enable may complete before the devices attached to the backplane link up following backplane initialization.
Steps To Reproduce: Perform controller reboot testing with an OEM specific NVMe backplane.

ID: SCGCQ01474266
Headline: The "pl reg" command dumps the wrong amount of data for some structures.
Description Of Change: Updated pl pci reg to dump valid registers by skipping reserved registers.
Updated to dump target mode dump when target mode is enabled.
Updated to get the correct amount of data for some structures along with minor changes to print some strings with fewer characters.
Issue Description: Dumping reserved registers in pl pci reg command. Dumping target mode data when target mode is not set. Dumping wrong amount of data for some structures.
Steps To Reproduce: Issues found by inspecting pl dbg output

ID: SCGCQ01478037
Headline: PL: SATA: Sense Key/Additional Sense code incorrectly set when open zone issued on a Security locked SMR drive
Description Of Change: Added a validation check of Locked device for Zone commands, except ReportZone, to now allow the command to be processed and instead fail with sense key set to ILLEGAL REQUEST and the additional sense code set to SECURITY CONFLICT IN TRANSLATED DEVICE as per SAT.
Issue Description: Validation check of Locked device for Zone commands, except ReportZone, was allowing the command to be processed.
Steps To Reproduce: Execute Open Zone command on a SMR drive which is security locked, the command fails with incorrect Sense Key/Additional Sense code.

ID: SCGCQ01445831 (Port Of Defect SCGCQ01418686)
Headline: Ventura/Marlin: NMI due to Host-side PCE credit starvation when there are simultaneous accesses to MSIX table and Generic Messaging Queue
Description Of Change: Turn off combined queue mode. This will limit the number of MSIX vectors to 16 and the 16 will be linearly mapped on AXI so they will match the host-view of MSIX tables. Turn off internal MSIX transfers and map the PCI Inbound Memory window to the AXI version of the MSIX vector table. Now that host reads and writes of the MSIX vector table are routed to AXI, the firmware will stall PCE AXI requests when accessing the associated Generic Message Queue register and then re-enable PCE AXI requests when done, thus avoiding the problem.

NOTE! This fix requires reconfiguration of the PCE core registers (i.e. the combined queue mode) and therefore requires a POR to take affect. In order to have immediate affect the user should download new firmware with the following NVDATA changes, preferable via UEFI, and then power cycle the card.
PceDword_00 00000000
DbiData_04 000FD011
DbiData_06 000FD011
Issue Description: If the host is constantly reading and updating the MSIX vector table at the same time that is sending MCTP or other VDM requests at a significant rate, it is possible that the firmware will attempt to free a Generic Messing Queue (VDM) queue entry withing one clock cycle of the host requesting a read of one of the MSIX table entries. On the rare occasion where this occurs, the host will not receive a completion resulting in a completion timeout from the host perspective. The firmware will also receive an external abort on the AXI bus and the PCE hardware will eventually send (after about 43milliseconds) a NON_FATAL error message. Credit will eventually run out from the host perspective and so, eventually, all activity will cease.
Steps To Reproduce: Read MSIX tables in bursts of 8 reads every 200 microseconds while simultaneously sending MCTP requests over PCI. After 5 to 48 hours the system may NMI when this condition hits.

ID: SCGCQ01474945 (Port Of Defect SCGCQ01471601)
Headline: VSES Target not added in host if event replay slot ordering is enabled.
Description Of Change: Add sending 'added' event for vSES device when slot order event replay is enabled.
Issue Description: If event replay slot order for direct attached devices is enabled in manufacturing page 7, while replaying the events firmware was only sending topology change list event for device connected to physical phys but not for vSES.
Steps To Reproduce: Flash Bios and Firmware on the controller card. Enable event replay slot order for direct attached devices in manufacturing page 7. Reboot the system. vSES target will not get added to host.

Defects Fixed (18):

ID: SCGCQ01201827

Headline: SAS Power Management and PCal do not work together

Description Of Change: SPICO firmware change to address interaction of periodic pcal and power management processes.

Issue Description: PHY takes a long time to enter partial slumber when power management timers are set to 2us - 100us.

Steps To Reproduce: Setup and Config details:
Intruder - Cub1 - Cub2 - PM capable SAS drives.
Slumber PM enabled on Cub-Cub link. PM is not enabled on Cub-Drive link.
Slumber timers set to 2uS.

It looks like both Cubs are sending Align0s after COMWAKE but none of them detect it.
Rx_Signal_Ok never asserts during this time. Eventually the SNLT timer expires and a link reset happens.

ID: SCGCQ01384089

Headline: Doorbell handshake hangs when faulted

Description Of Change: Once we fault, we handle interrupts by polling.
Any interrupts we wish to handle in this state must be configured to allow us to recognize them when polling.
The FIQ interrupt for the Doorbell was not being changed, so code was added to configure it properly when we fault.

Issue Description: After some faults, it is still possible to use a MPI TOOLBOX command through the Doorbell to send and receive CLI commands and responses.
In the latest loads this functionality is not working - once the controller is faulted, there is no response to Doorbell.

Steps To Reproduce: 1) Fault the controller, either with the CLI or through the Doorbell.
2) Send TOOLBOX CLI commands through the doorbell and look for proper responses.

ID: SCGCQ01421447

Headline: Drive missing on power cycle

Description Of Change: Throughout the processing of spin up requests, the firmware re-reads the register which reports the phys that are requesting spin ups. If the value changes in the middle of the processing, the firmware may inadvertently clear a request that it has not yet processed. The change is to take a snapshot at the beginning of the processing and use it throughout all the processing. If a new request arrives, it will get picked up the next cycle.

Issue Description: Sometimes a drive is missing or takes a long time to show up after a power cycle.

Steps To Reproduce: Do I/Os to all of drives for a while and start power cycle.
Every time enter OS the script will check the num of drives, if it finds there are drives missing, the script would stop and record the reason of exiting.

ID: SCGCQ01439249

Headline: File name capitalization doesn't match #include and fails when building with Linux

Description Of Change: Changed the capitalization of the libBaseTypes.h file in api directory to match the case used in the header file.

Issue Description: There is an include file with the wrong case spelling:
gen3base/comboserdeslib/api/libBasetypes.h

where it's included in
gen3base/comboserdeslib/api/aviSerdes.h as:
#include "libBaseTypes.h"

Steps To Reproduce: N/A

ID: SCGCQ01450399

Headline: PL trying to perform memory move using address which is in the non-addressable range

Description Of Change: The original message is saved prior to it being overwritten to process the request. When the request is aborted, the original message is restored. The incorrect size was being used to save and restore the message and therefore the original SGL was lost in the process. The entire message frame size is now being used to save and restore the message.

Issue Description: SATA passthrough command is using bad address when moving data from drive to destination buffer.

Steps To Reproduce: Issue SATA Passthrough command.
Issue TM to abort it.
Re-issue the same message frame.

ID: SCGCQ01451022

Headline: vSES Target: Allocation Length less than 16 Bytes for REPORT LUNS Command is not Handled Properly

Description Of Change: In case of allocation length is less than 16, instead of failing firmware now sends as much data as requested by the Report LUNs command.

Issue Description: Report LUNs command sent to vSES target with allocation length less than 16 was being failed by the firmware with check condition. As per spec it should send the requested amount of data.

Steps To Reproduce: Send SCSI Report Luns command to vSES target with allocation length less than 16, the command will get failed with check condition.

ID: SCGCQ01451678

Headline: vSES Target: Incorrect Sense Data for REQUEST SENSE Command

Description Of Change: Initialize the sense data stored for vSES device to sense key set to no sense and ASC/ASCQ set to 0 with error code set to 'response code current' and remove storing of sense data that was already sent.

Issue Description: For vSES device firmware was sometimes sending incorrect sense data.

Steps To Reproduce: Send the Request Sense SCSI command to the vSES device, sometimes f/w will return the incorrect sense data.

ID: SCGCQ01455651

Headline: pl: backend PCIe: erroneous address pool copy

Description Of Change: Fixed a bug that could cause unexpected replication of start of day backend PCIe address space configuration information.

Issue Description: If the IOC_CFG_EXT_MFG_44_ALLOC_FLAGS_MODE_BAR_FALL flag is set in Extended Manufacturing Page 44, a sequence of events may occur that causes address pool information to be copied multiple times into a PL data structure when it is expected to be copied only once.

Steps To Reproduce: Code inspection.

ID: SCGCQ01455680

Headline: pl: port enable may fail to complete if an OEM backplane is attached

Description Of Change: Ensure that backplane initialization is complete before device presence polling is enabled.

Issue Description: If a specific OEM backplane with NVMe support is attached to the controller, the backplane initialization routine may malfunction, causing port enable to fail to complete.

Steps To Reproduce: Attach a specific OEM backplane to the controller and bring up firmware.

ID: SCGCQ01456349

Headline: Ventura: Break up backplane mgmt device ISTWI Read/Write to the supported size

Description Of Change: Modified FW to break up multi byte ISTWI Read/Write IO to a backplane mgmt. device in to max supported size transfers.

Issue Description: Some of the NVMe backplane mgmt. devices seems to support max Read/Write length of WORD (16-bits) in a transaction and sending multiple byte write may not update appropriate register offsets so break up the multi-byte ISTWI request to max support size tranfers.

Steps To Reproduce: n/a

ID: SCGCQ01463496

Headline: Hot plugged NVMe drive fails to link up on OEM backplanes with ISTWI drive presence polling enabled

Description Of Change: Modified PL FW to keep PCIe Reset (PERST#) in asserted state for empty slots and perform PCIe reset sequence on hot-plug drive presence detection.

Issue Description: During tri-mode backplane detection, the PL FW deasserts the PERST# on for all slots but on a NVMe drive is hot-plug, FW do not seem to perform PCIe reset sequence and due to this, the hot-plugged NVMe drive do not link up.

Steps To Reproduce: Connect 9400-16i HBA to ISTWI drive presence polling supported OEM backplane with no drives populated.
After controller FW initialization, insert a NVMe drive and observe no link up of drive or discovery.

ID: SCGCQ01465058

Headline: Ventura: Firmware Update Algorithm Frees Mids Twice

Description Of Change: Fixed the mid-tracking math so that the correct mids are added to the free queue

Issue Description: When the BIOS memory is freed some mids are freed twice resulting in IO errors

Steps To Reproduce: Run the development tip (not released)

ID: SCGCQ01468144

Headline: pl: NVMe: 6001 fault

Description Of Change: Fixed an issue that caused an IO to not be aborted if it was found on an internal exception queue while handling an Abort Task.

Issue Description: If an Abort Task task management request is sent to an NVMe device, it may unexpectedly fail to abort the targeted IO. When a device reset class task management request is then sent to the device, a 6001 fault will occur.

Steps To Reproduce: Repeatedly send Abort Task task management requests to an NVMe device while issuing heavy firmware translation path IO to the device.

ID: SCGCQ01470385

Headline: To support the I2C bus reserve state in the case of UBM backplane

Description Of Change: The i2c bus reserve state change done to the UBM back plane case as well.

Issue Description: In order to align with the main line changes where the other back planes support i2c bus reserve state, similarly the change needs to be done for the UBM back plane.

Steps To Reproduce: NA

ID: SCGCQ01341898 (Port Of Defect SCGCQ01333993)

Headline: PL : performance drop of nearly 40% in sequential write and seqential Reads

Description Of Change: Corrected the condition check so that all the entries in the spin up queue are traversed while checking for clearing the spin up falling edge interrupt

Issue Description: While iterating through the spin up request queue to check and clear Spin up falling edge interrupt, the head entry is missed and
spin up falling edge interrupt was not getting cleared.
Due to this spin up handler was called repeatedly.
Performance drop was observed because of this.

Steps To Reproduce: Run performance runs on widows OS with 2 drive RAID 0 (WB/DIO/DCD) with 24 Direct attached drives.

ID: SCGCQ01385320 (Port Of Defect SCGCQ01358138)

Headline: PL : Drives may not spin up due to bug in spin up path found during code walk through

Description Of Change: Corrected the check so that spin up queue is iterated through all the entries.
The last entry is not missed.

Issue Description: The last entry is missed while iterating through the spin up queue.
The loop starts with the next node and iterates till the next node is NULL.
So the last entry is always missed.

Steps To Reproduce: NA

ID: SCGCQ01458074 (Port Of Defect SCGCQ01330984)

Headline: PL : PWR_GRANT is not issued upon PWR_REQ from SPL2 drive

Description Of Change: While processing spinup request, check the SAS Address and device type of identify frame, if it has reset values then skip processing the request as the identify frame data is invalid.

Issue Description: PWR_GRANT is not issued upon PWR_REQ from SPL2 drive

Issue sequence:
1. Identify frame is received, PWR_REQ has come and interrupt is set.
2. Link change, FW clears identify frame data in internal structure
3. Spinup request is processed and power capability in identify frame is referred which is already cleared by FW.

This misleads to detect an SPL2 drive as legacy SAS. Hence PWR_GRANT is not sent.

Steps To Reproduce: 1. SPL2 compliant drives are connected.
2. There should be a link reset sequence after initial identify frames are received and before spinup request is handled.

ID: SCGCQ01458664 (Port Of Defect SCGCQ01455200)

Headline: PL : PL fault 0x7C72 is hit during discovery when disabling and enabling all the PHYs connected to legacy SAS drives

Description Of Change: Updated periodic notify queue pointers correctly when all the entries are removed from the queue

Issue Description: After legacy SAS drives spinup, NOTIFY primitive should be sent periodically.
This is done by maintaining periodic notify queue in firmware.
If all the phys are connected with legacy SAS drives, the queue becomes full.
Later when all the phys are disabled, the entries are removed from the queue but the queue pointers are not updated properly.
When the phys are re enabled, the periodic notify queue is found full even though its empty as pointers are not updated.
This leads to 0x7C72 fault.

Steps To Reproduce: 1. Connect all the controller phys to legacy SAS drives.
2. Disable and enable the phys.
3. 0x7C72 fault is hit.

Enhancements Implemented (27):

ID: SCGCQ00922883

Headline: Ventura: Remove VENTURA_PORTING from Makefiles and headers

Description Of Change: Clean up code from integration activities.

ID: SCGCQ00922893

Headline: Ventura: Remove VENTURA_PORTING from ARM Initialization/Utilities.

Description Of Change: Remove comments and fix any code sections that were identified as areas to adjust during initial porting of code to Ventura platforms.

ID: SCGCQ01230723

Headline: Ventura: Move firmware update copy process to main firmware to avoid PCE problems

Description Of Change: Move backup to main firmware update process into the last stage of the boot process (main firmware). Moving the images in the background allows the PCE root complex to send config cycles and read the FMU more quickly.

ID: SCGCQ01276256

Headline: MPI 2.6: Device side PCIe SRNS flag

Description Of Change: Added SRNS support to the LinkFlags field of the PhyData structure in PCIe IO Unit Page 1.

ID: SCGCQ01305760

Headline: MPI 2.6: Add new firmware download type (CPLD IMAGE)

Description Of Change: Added CPLD image type to Firmware Download Request Message.

ID: SCGCQ01328437

Headline: Ventura: Enclosure Mgmt optimizations and enhancements

Description Of Change: This Enhancement mainly involves Enclosure Mgmt. optimizations.
- To process queued SEP requests in a proper way to avoid stack overflow.
- Combine the SEP request completion in to a function.
- Optimize SGPIO registers configuration during init.
- Also add UART CLI I2C debug commands to read/write to I2C devices registers.

ID: SCGCQ01339864

Headline: MPI 2.6: add NVMe SGL Data Block descriptor alignment flag

Description Of Change: Added MPI26_PCIEDEV2_CAP_DATA_BLK_ALIGN_AND_GRAN to the Capabilities field of PCIe Device Page 2.

ID: SCGCQ01373008

Headline: MPI 2.6: Add Aero PCI Device IDs

Description Of Change: Added PCI Device IDs for Aero.

ID: SCGCQ01394882

Headline: Reduced amount of data in pl dbg trace output

Description Of Change: Removed prints of reserved registers and trailing Dwords of zeros on frames

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ID: SCGCQ01412195

Headline: To read the port Capabilities from backplane implementing UBM and to validate backplane configuration

Description Of Change: The port capabilities of the UBM supported backplane read per backplane management device. This is validated to find the valid backplane configuration.

ID: SCGCQ01412198

Headline: Enable I2C polling for drive presence detection in UBM backplanes with NVMe support.

Description Of Change: Firmware uses I2C polling to check for NVMe drive presence in UBM backplane and if drive presence is detected PERST is controlled accordingly.

ID: SCGCQ01412209

Headline: Controlling Slot Locate/Fault LEDs in a backplane which implements UBM.

Description Of Change: This supports the slot control functionality of Locate/fault LEDs for the UBM supported backplane.

ID: SCGCQ01416498

Headline: MPI 2.6: Add ControllerResetTO to PCIe Device Page 2

Description Of Change: Added ControllerResetTO field to PCIe Device Page 2.

ID: SCGCQ01416515

Headline: MPI 2.6: Add new reason code to PCIE Device Status Change Event

Description Of Change: Added MPI26_EVENT_PCIDEV_STAT_RC_PCIE_HOT_RESET_FAILED to the ReasonCode field in PCIe Device Status Change Event Data.

ID: SCGCQ01430672

Headline: Ventura: NVMe 1.3 Support: Firmware Update Granularity

Description Of Change: Firmware Update Granularity (FWUG) field indicates the minimum granularity and alignment of the data provided in the Firmware Image update command.
The data provided in the command should conform to the Firmware Update Granularity indicated in the device's Identify Controller data structure.
New functionality will indicate an error status to host when it tries to violate the granularity and alignment requirements.

ID: SCGCQ01430674

Headline: Ventura: NVMe 1.3 Support: Namespace Optimal IO Boundary

Description Of Change: Added a support to expose the Namespace Optimal IO Boundary(NOIOB) for a namespace to host. Host software can use this value when constructing the read and write commands that do not cross the IO boundary to achieve optimal performance.

ID: SCGCQ01445877

Headline: PL: Add firmware support for depopulation of SATA drives

Description Of Change: Depopulation features allows drives with single platter failure to be reconfigured with lower capacity and avoid having to replace entire drive. This code enables depopulation support for SATA drives which are capable of this feature. It does identify such drives during SATA Init process and adds support for SATA translation of specific commands to facilitate this functionality.

ID: SCGCQ01445903

Headline: pl: NVMe: NVMe task management modifications (part 2)

Description Of Change: A couple more modifications related to NVMe task management for improved robustness and compatibility with NVMe devices.

ID: SCGCQ01448575

Headline: Reduce time taken by host to initialize one SATA drive.

Description Of Change: Firmware pends any IOs received while SATA drive is not initialized by the firmware and then check and starts the pended IO in a timer callback every 250 ms. With this change firmware will start the pended IO as soon as SATA initialization completes, instead of waiting for timer callback. Also reduce the frequency of checking and starting pended IOs from 250 ms to 1/16th of a second.

ID: SCGCQ01449138

Headline: MPI 2.6: PCIe Device Page 2 reporting Namespace Optimal IO Boundary(NOIOB) for NVMe devices

Description Of Change: Added Namespace Optimal IO Boundary (NOIOB) field to PCIe Device Page 2.

ID: SCGCQ01454612

Headline: Ventura: Re-order pl dbg to put most useful, less verbose prints first

Description Of Change: Since people often neglect to disable adapter resets when collecting pl dbg, move some of the more critical yet less verbose prints such as pl task and pl eminfo before prints that spit out lots of hex dumps to increase the likelihood of getting them on the first try.

ID: SCGCQ01462690
Headline: Ventura: Change iopiDiagCmdReadMem() to not print rows of zeros
Description Of Change: In order to reduce the time to dump debug data such as "pl dbg", detect rows of zero and skip printing them. Instead, print the count of zero dwords detected. For example:
F0B00090: [0's: 24]

ID: SCGCQ01464914
Headline: Ventura: Modify plDiagCmdShowRegister() to skip printing of dwords of 0 when regSize == 4.
Description Of Change: In order to reduce the time to dump debug data such as "pl dbg", detect rows of zero and skip printing them. Instead, print the count of zero dwords detected. For example:
F0B00090: [0's: 24]
Also stop printing leading zeros beyond the field size for DevHandle, MID & SASCore.

ID: SCGCQ01464951
Headline: PL: Add NVDATA option to gracefully handle invalid BP Type configurations
Description Of Change: Added new flag to Man Page 6 GPIO that will allow the controller FW to gracefully handle some invalid configurations without faulting.

ID: SCGCQ01465016
Headline: pl: backend PCIe: reduce firmware initiated PCIe transaction wait time
Description Of Change: PL handles completion of firmware-initiated PCIe transactions more quickly.

ID: SCGCQ01468138
Headline: Skipping additional reserved registers when printing pl dbg trace
Description Of Change: skipping reserved registers and non sas core reserved registers.

ID: SCGCQ01458359 (Port Of EnhancementRequest SCGCQ00870423)
Headline: PL:Move ownership of SES Page 0x0A slot mapping from devices to PHYs
Description Of Change: Modify the SES Page 0x0A handling such that the slot mapping is done with the PHY index instead of the Device. This will ensure that the slot status updates are available even if no device exists in the slot.

ReleaseOrder ID:	*SCGCQ01458609* Open In CQWeb
Headline:	*Ventura IT: SASFW_Ventura - 05.250.00.00 Firmware*
Release Version:	*05.250.00.00*
UCM Project:	*SAS3.5FW_MASTER_DEV*
Sub UCM Project:	*SASFW_Ventura_Phase_6.0*
UCM Stream:	*SASFW_Ventura_Rel*
Release Type:	*Pre-Alpha*
State:	*Superseded*
Release Baseline:	*SASFW_Ventura-2017-09-25-05.250.00.00_REL_1506379242@ \SAS_CTRL_FW*
Release Date:	*12-OCT-17*
Date Generated:	*Feb 16, 2018*

Defects Fixed (30):

ID: SCGCQ01294948
Headline: pl: backend PCIe: E984, E9A4, EF50, EF52 faults
Description Of Change: Prevent an issue where part of the root port gets stuck during hot reset or link down handling.
Issue Description: If a hot reset or surprise down occurs on a device side PCIe link with heavy IO running to the devices attached to the link, an E984, E9A4, EF50, or EF52 fault may occur.
Steps To Reproduce: Perform link glitch testing on device side PCIe links while running heavy traffic through them.

ID: SCGCQ01312345
Headline: pl: backend PCIe: ECE4 fault
Description Of Change: Default to Fatal severity if the severity of an error indicated by a backend PCIe device cannot be determined.
Issue Description: If an NVMe device generates a PCIe fatal or nonfatal error message but then indicates that no errors have happened, an ECE4 fault may occur.
Steps To Reproduce: Perform PCIe link glitch and link break testing with various NVMe devices.

ID: SCGCQ01352937
Headline: pl: NVMe: missing AccessStatus codes
Description Of Change: If NVMe device initialization persistently fails due to an NVMe register access failure, idle timeout, or Controller Fatal Status, report the corresponding AccessStatus.
Issue Description: There are a few PCIe Device Page 0 AccessStatus codes that should be reported when NVMe device initialization persistently fails for the corresponding reason that aren't being reported.
Steps To Reproduce: Code inspection.

ID: SCGCQ01373888
Headline: Ventura SBR: Changes to PLL reset requirements cause lock failure on some boards
Description Of Change: Change a mux setting to allow the proper PLL signal through.
Some reset conditions seem to cause this mux to select the wrong default output.
Issue Description: Specific boards are unable to connect to the host system when they are loaded with an RMC that contains the latest PLL reset algorithm.
This algorithm added the disable and then enable of the PCE PLL during reset. Previously the RMC was only resetting the PCE PLL.
On a small subset of boards, this change causes the host not to recognize the board during boot (no PCIe link is established)
Steps To Reproduce: Power on board and observe that it is not detected by host.

ID: SCGCQ01377242
Headline: PL: More than one ATA command at a time may be submitted to a SATA device
Description Of Change: The drive will be reset when SATA init times out.
Issue Description: If a SATA device takes more than three seconds to respond to a ATA command during SATA Initialization the controller may restart SATA Init. When the device returns data from the initial ATA command the controller will misinterpret the data.
Steps To Reproduce: 1. Insert a drive into the topology.
2. Cause a ATA command submitted by the controller to take longer than three seconds.
3. When new ATA commands start getting issued to the drive cause the drive to return the data from step 2.

The actual behavior is variable as it depends on outstanding commands and the controller's internal state.

ID: SCGCQ01390095
Headline: IOP: Improvements to AXI HWWA
Description Of Change: Improvements to the firmware to win Bus Arbitration
Increased the number of attempts and also changed the address to improve the chances of winning Arbitration
Issue Description: I2C DMA and I2C arbitration was lost and the firmware locked up.
Steps To Reproduce: Do reboot cycles continuously until firmware either faults (0x0906) or locks up.

ID: SCGCQ01392675
Headline: Ventura B0: Missing signing supported firmware image in RO
Description Of Change: Modified Ventura release script to build and include signing supported firmware image in the release order.
Issue Description: Signing supported firmware image is missing in the release order.
Steps To Reproduce: Run the release script, it does not build sign firmware images.

ID: SCGCQ01394426
Headline: PCI SIG Compliance Test Failure - Test 1_8 Virtual Channel
Description Of Change: Corrected the PCE SBR setting to have Resizable BAR capability at PCIe configuration space offset 0x3cc
Issue Description: For the 3616 controller based board , IT firmware advertised Virtual Channel/Virtual Traffic capability at offset 0x3cc of pcie configuration space instead of Re sizable BAR capability , which lead to the PCI SIG compliance test failure.
Steps To Reproduce: - Start PCIECV.EXE test application on Windows 7 32-bit OS with 3616 controller based board in system.
- run test 1_8

ID: SCGCQ01394478
Headline: PCI SIG Compliance Test Failure - Test 1_41 Link Capabilities 2, Link Control 2, Link Status 2 Failures
Description Of Change: Hardware setting RunDbilsmOnWarmReset interferes with the existing workaround for "sticky bits" in the PCIe config space.
Disable this setting and the bits perform as expected.
Hardware analysis determined that there were no negative impacts from clearing this bit.
Issue Description: During PCIECV Configuration Space compliance testing, test 1_41 Link Capabilities 2/Link Control 2/Link Status 2 fails on Mercator with production firmware 4.00.00.00.

Steps To Reproduce: Perform specified test.

ID: SCGCQ01397553
Headline: Customer specific SAS 12g drive frequently links up at 6g.
Description Of Change: Modified SPICO firmware detection of tx_init transition of attached device. This change is the only change from the previous 6069 version. It has been validated by analog test process, but has not been through a software test cycle.
Issue Description: Customer specific SAS 12g drive frequently links up at 6g
Steps To Reproduce: Direct attach customer 12g SSD device to any controller phy and initiate link reset.

ID: SCGCQ01412908
Headline: Ventura: NVMe Target: Non-Zero Value in TRACK SKEW FACTOR field of FORMAT DEVICE Mode Page
Description Of Change: TRACK SKEW FACTOR parameter in FORMAT DEVICE Mode Page of NVMe target was zeroed out.
Issue Description: TRACK SKEW FACTOR parameter in FORMAT DEVICE Mode Page of NVMe target was non zero.
Steps To Reproduce: Run this sg_util command: sg_raw -r 512 /dev/sg2 1a 00 03 00 ff 00 -vvv
And check TRACK SKEW FACTOR parameter.

ID: SCGCQ01414966
Headline: pl: NVMe: async event persistent conditions monitor issues
Description Of Change: Fixed some issues related to the NVMe asynchronous event persistent conditions monitor.
Issue Description: Some issues with the NVMe asynchronous event persistent conditions monitor were identified thru review.
Steps To Reproduce: Code inspection.

ID: SCGCQ01415544
Headline: Internal Task Management operations not completing in out of resource conditions
Description Of Change: The change is to reuse the resource that the Task Management used to send the TM completion event.
Issue Description: Internal Task Managements can run almost to completion but will not complete and free up the resources used for that operation because the firmware is waiting on one more resource to send a completion event. If all the system resources are tied up it's possible to get into a deadlock as no processes can move forward.
Steps To Reproduce: Do cable push/pull testing on a large topology with IOs going.

ID: SCGCQ01416481
Headline: 0x6004 Fault during TM injection while running IO to Sata SSDs.
Description Of Change: When restarting the next portion of a unmap/trim command and there is an outstanding TM for that device, increment IO count when it's added to the abort list to keep all the counters in sync.
Issue Description: If an unmap command is in progress when a TM is active, the unmap command can be added to the abort list, but the running IoCount doesn't take that IO into account, so the number of aborted IOs could be larger than the IOCount when the TM completes.
Steps To Reproduce: Issue Target Reset to devices while running IOs, including unmap/trim.

ID: SCGCQ01418575
Headline: When disabling one phy of a port the other phys of the same port do not relink after reset.
Description Of Change: Added validation of DisablePhy bits during port configuration. If PCIe support is also enabled on the phy, then all the phys within a link configuration must have the same setting for DisablePhy bit. If they are not, an error status is returned to port enable.
Issue Description: After setting the DisablePhy bit for some phys in SAS IO Unit page 1 and resetting the controller, attached SAS devices are no longer detected on other phys.
Steps To Reproduce: 1) Connect one port of the controller to the enclosure/expander
2) Disable one of the phys that's connected to the enclosure (modifying sas io unit page 1)
3) Issue a diag reset after disabling the phy.
4) After the issuing the diag reset all the devices connected to the port gets removed.
5) Enabling the above disabled phy makes all the phys online and the devices gets added back.

Only occurs if PCIe is also enabled for the phy.

ID: SCGCQ01428178
Headline: Add SAS device discovery error event to IOP message events.
Description Of Change: Added SAS device discovery error event to IOP message events in iopMsgEvents file.
Issue Description: Add SAS device discovery error event to IOP message events.
Steps To Reproduce: 1. Use expanders setup and jamming SMPs going to various expanders.
2. When SMP failed on one of the expander, event is getting sent by the FW.
3. FW is not sending events.

ID: SCGCQ01428718
Headline: Ventura: Misc tri-mode backplane mgmt detection fixes and Slot status update changes
Description Of Change: Updated FW to use correct backplane device register offsets during backplane detection and changed slot status updates to write only for backplanes that do not report current slot status.
Issue Description: Use correct backplane device register offsets during backplane detection and restrict the slot status updates to write only for backplanes that do not report current slot status.
Steps To Reproduce: n/a

ID: SCGCQ01429439
Headline: 9405W-16i xml not available in Latest Release Order
Description Of Change: Added 9405W-16i xmls to the FW release
Issue Description: 9405W-16i xml not available in release order (SCGCQ01422232)
Steps To Reproduce: n/a

ID: SCGCQ01429659

Headline:	pl: NVMe: memory leak in Verify (10/12/16) command translation
Description Of Change:	Properly clean up memory allocated for a Verify command translation.
Issue Description:	Some IOC-local memory is allocated for translation of a Verify (10/12/16) command but it may not be freed.
Steps To Reproduce:	Issue SCSI Verify commands to NVMe devices while monitoring per-device IOC memory usage.

ID:	SCGCQ01435884
Headline:	pl: Mode Select translation transfer length validation
Description Of Change:	Validate the provided transfer length when translating a SCSI Mode Select command.
Issue Description:	The Mode Select command translations for SATA and NVMe should validate the provided transfer length.
Steps To Reproduce:	N/A

ID:	SCGCQ01444725
Headline:	Ventura: NVMe Target: REPORT LUNS SCSI Command Failed With CC for Supported SELECT REPORT field Values 01h, 10h or 12h
Description Of Change:	For the REPORT LUNS SCSI Command with SELECT REPORT field Values 01h, 10h or 12h , firmware is sending minimum bytes of data and completing the command with successful status .
Issue Description:	For the REPORT LUNS SCSI Command with SELECT REPORT field Values 01h, 10h or 12h , firmware is not returning any data and fails the command.
Steps To Reproduce:	Send REPORT LUNS SCSI Command with SELECT REPORT field Values 01h , 10h or 12h to the NVMe drive connected to Ventura controller.

ID:	SCGCQ01444843
Headline:	Ventura: NVMe Target: When MODE SENSE Command Executed for all supported Modes Pages, TRACK SKEW FACTOR Set as 0x01
Description Of Change:	Zeroed out TRACK SKEW FACTOR when reading all supported mode pages.
Issue Description:	Execute a MODE SENSE SCSI Command to NVMe target for reading all supported mode page details, the command passed with data returned. But TRACK SKEW FACTOR is not set as Zero for FORMAT DEVICE Mode Page.
Steps To Reproduce:	Run following sg utils command to get all mode pages from NVMe drive: sg_modes /dev/sg2 -v

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ID:	SCGCQ01448015
Headline:	GoldenX: When no BIOS option is selected the images are 1MB too small
Description Of Change:	Added code to fill the unspecified BIOS image area
Issue Description:	If one doesn't specify BIOS images to add to an image the size of the flash image is too small
Steps To Reproduce:	goldenx <firmware>

ID:	SCGCQ01449239
Headline:	A previous code change is missing a few changes.
Description Of Change:	Added the missing lines of code.
Issue Description:	A few lines of code were missing from changes checked into SCGCQ01415544.
Steps To Reproduce:	This was found by inspection while CSET'ing the changes in SCGCQ01415544.

ID:	SCGCQ01450475
Headline:	Get VDM Support command does not have VendorID and VendorAddInfo fields properly populated
Description Of Change:	VendorId is populated correctly now.
Issue Description:	VendorId is not populated correctly.
Steps To Reproduce:	1) Update the controller with Ventura Main. 2) From BMC try pulling VendorDefined Message Support. 3) observe that vedorId is not correct.

ID:	SCGCQ01451332
Headline:	pl: NVMe: EC26 fault
Description Of Change:	Fixed an issue that broke handling of a completion queue entry with the More bit set.
Issue Description:	If an NVMe device throws a medium error, and the More (M) bit is set in the completion queue entry associated with the failed command, an EC26 fault will occur.
Steps To Reproduce:	Perform NVMe device media error injection testing.

ID:	SCGCQ01411982 (Port Of Defect SCGCQ01295414)
Headline:	PL Discovery: After Port Down, Expander Is Not Removed and Firmware Retries SMP Indefinitely
Description Of Change:	Fixed a couple of bugs in the discovery callback code which handles SMP responses.
Issue Description:	After port down due to powering off expanders and drives, some expanders are still shown in controller CLI pl status. Upon examination of firmware trace buffer, firmware is stuck repeatedly trying to send an SMP on the down port. This appears to continue indefinitely and the expanders are never removed.
Steps To Reproduce:	1. With a large topology of many expanders and drives, run IO to all drives. 2. While running heavy IO, power off the expanders and drives. 3. If the issue is reproduced, some expanders will still appear in CLI pl status command, long after they should have been removed.

ID:	SCGCQ01442629 (Port Of Defect SCGCQ01438119)
Headline:	Ventura vSES: SAS and SATA direct attached devices are not getting associated to vSES in Windows Storage Spaces Direct.
Description Of Change:	Set the SAS address field in phy descriptor of additional element status descriptor correctly for the end device. Send SAS address as one of the device id descriptor in vpd page 0x83 for SATA device if vSES is enabled.
Issue Description:	1. The SAS address of the direct attached end devices is populated in phy descriptor of Additional Element Status descriptor in the Additional element status diagnostic page (pagecode 0x0A). Firmware was incorrectly filling this value with SAS address of the phy the device is attached to. 2. Inquiry command send to SATA drive with vpd page set to Device Id (pagecode 0x83) was not returning the SAS address of the device as one of the device id descriptor.
Steps To Reproduce:	Attach a few SAS and SATA drives directly to the controller and run following commands in windows powershell. 1. Get-StorageFaultDomain -Type PhysicalDisk 2. Get-StorageFaultDomain -Type StorageEnclosure | Get-StorageFaultDomain -Type PhysicalDisk | fl * a) Cmd 1 should show SATA's PhysicalLocation to be Slot. b) Cmd 2 should show SATA drive info.

ID:	SCGCQ01442976 (Port Of Defect SCGCQ01417361)
Headline:	Customer experiences 5-7 % performance drop on 24 direct connected SAS SSD R10/R6 setup.
Description Of Change:	Removed the debug print from the fast path completion handler.
Issue Description:	A debug print in Fast path completion handler introduces 5-7 % performance drop.
Steps To Reproduce:	Perform I/O(Read/Write) using iometer with different Queue depths(ranging from 4 256).

ID:	SCGCQ01451191 (Port Of Defect SCGCQ01445053)
Headline:	Microsoft S2D Verify IO with CSV Move fails direct attached Enclosure validation on 94xx HBA's
Description Of Change:	Modified FW to provide the necessary VSES VPD page 83h device identification data.
Issue Description:	Microsoft S2D Verify IO with CSV Move fails direct attached Enclosure validation on 94xx HBA's due to non-availability of required device identification data from VSES VPD page 83h.
Steps To Reproduce:	Run S2D Verify IO with CSV Move test with cluster setup on 9400-16i HBA.

Enhancements Implemented (13):

ID: SCGCQ01240422

Headline: Ventura/Marlin: When the SPICO code fails checksum, Patch SPICO Signature and Checksum

Description Of Change: When the SPICO code fails to pass hardware checksum and yet the SPICO signature is good, the SPICO hardware will not bring the host interface up on the PCIe bus.   This change is a modification to the previous fix. In addition to invalidating the SPICO signature, this re-enables the checksum so that the CBB is verified on every pass.

ID: SCGCQ01275066

Headline: pl: NVMe: support for devices with large sector sizes

Description Of Change: Made some PL changes to enable support for NVMe devices with large sector sizes.

ID: SCGCQ01412194

Headline: Ventura B0:(UBM) Identifying a UBM Capable backplane

Description Of Change: Add support to detect a UBM capable backplane.

ID: SCGCQ01419083

Headline: pl: NVMe: NVMe task management modifications

Description Of Change: Some modifications to NVMe task management for improved robustness and compatibility with NVMe devices.

ID: SCGCQ01431067

Headline: pl: NVMe: IO breakup structure modification

Description Of Change: Modified a member of a PL internal data structure used during NVMe IO breakup. There should be no externally visible changes from this modification.

ID: SCGCQ01434061

Headline: Ventura: NVME 1.3 Support: Add new Status Codes to header files

Description Of Change: Change NVME_SC_RESERVED1 to Operation Denied. Review other SC's added to 1.3 and add them all to nvmeProtocol.h.

ID: SCGCQ01436612

Headline: pl: NVMe: don't require a resource frame for some SCSI-NVMe translations

Description Of Change: Use an existing statically allocated buffer for SCSI-NVMe translation where possible. This is a PL optimization that should not cause any externally visible changes.

ID: SCGCQ01440247

Headline: pl: NVMe: SGL translation performance tweaks

Description Of Change: Made a couple of tweaks that may improve NVMe SGL translation performance with some workloads.

ID: SCGCQ01448576

Headline: (SATA Only) Add support for SCSI Read Capacity command when drive is in spun down mode.

Description Of Change: Read capacity, Read Capacity (16), Mode Sense and Mode Sense (10) SCSI commands send to SATA drive while it is in spun down mode will not be failed but translated as per sat spec.

ID: SCGCQ01449325

Headline: Ventura/Marlin: Add support for Winbond 256Mbit SPI FLASH

Description Of Change: Add support for the Winbond W25Q256JW part

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ID: SCGCQ01454125

Headline: (SATA Only) Add support for NDOB bit in translation of SCSI Write Same Command to SATA drives

Description Of Change: When NDOB bit is set no data is sent along with SCSI Write SAME (16) command. In most cases it translates to writing zeros to specified range of LBAs on the drive. Writing zeros is done using ZERO EXT, SCT Write Same or Write ATA commands depending on what the drive supports.
Also according to latest SAT spec proposal SCSI Write same does not translate to DATA Set Management (Trim) command if 'Unmap' bit is set instead it uses 'Trim' feature in ZERO EXT command if drive supports it.

ID: SCGCQ01429867 (Port Of EnhancementRequest SCGCQ01429655)

Headline: PL: Change avoid duplicate mid LUN reset option to abort task set

Description Of Change: For the avoid duplicate mid feature, changed the LUN reset option to abort task set.

ID: SCGCQ01436959 (Port Of EnhancementRequest SCGCQ01404241)

Headline: Ventura VSES: Unique id and serial number for virtual SES to support microsoft storage spaces direct.

Description Of Change: Use enclosure's logical id sas address to program the unique id in Device identification VPD page (page code 0x83) and unit serial number VPD page (page code 0x80).