Change Summary (Defects=2 Enhancements=2)

SCGCQ00453641 (DFCT) - File system creation on a SATA SSD drive failed in Linux.
SCGCQ00459862 (CSET) - IOP: Value of PCIe SERDES parameter causes less than optimal margin
SCGCQ00459855 (CSET) - Use Dual Contexts in Tx Context Manager Only When Expanders Are Present
SCGCQ00459856 (CSET) - IOP: Update PCIe SERDES with improved settings

Total Defects Resolved (2)

(SCGCQ00453641)	*Defect 1/2*
HEADLINE:	File system creation on a SATA SSD drive failed in Linux.
DESC OF CHANGE:	Modified the values for the UNMAP parameters reported in the Block Limits VPD page so as to allow the host to send down UNMAP commands with high LBA count.
TO REPRODUCE:	Attach a SATA SSD drive of at least 200 GB capacity to the controller on a Linux host. Issue mkfs.ext4 command to create a file system on the drive. Observe the command timing out.
ISSUE DESC:	File System creation on a SATA SSD drive failed in Linux.

(SCGCQ00459862 - Port of SCGCQ00400449)	*Defect 2/2*
HEADLINE:	IOP: Value of PCIe SERDES parameter causes less than optimal margin
DESC OF CHANGE:	Modified the PGLIM parameter in the PCI-Express SERDES to a value determined by Systems Engineering to improve margin.
TO REPRODUCE:	Not applicable
ISSUE DESC:	The default value of a PCI-Express SERDES register has been found to cause less than optimal margin on certain bench tests. The default value does not violate specs, but the value is less than optimal.

Total Enhancements Implemented (2)

(SCGCQ00459855 - Port of SCGCQ00419356)	*Enhancement 1/2*
HEADLINE:	Use Dual Contexts in Tx Context Manager Only When Expanders Are Present
NEW FUNCTIONALITY:	Dual Contexts in Tx Context Manager will only be used when expanders are present in the topology. If only direct attach high performance drives are present, performance is best without the dual contexts setting enabled.

(SCGCQ00459856 - Port of SCGCQ00408335)	*Enhancement 2/2*
HEADLINE:	IOP: Update PCIe SERDES with improved settings
NEW FUNCTIONALITY:	Added code to modify the PCIe core SERDES values to the parameters recommended by the analog team and tested by the System Engineering team. These changes are only done for C0 silicon.

Change Summary (Defects=3 Enhancements=2 NVDATA=3)

SCGCQ00437674 (DFCT) - Default NVDATA for Gen 3 uses wrong SGPIO clock divider
SCGCQ00440212 (DFCT) - Update NVDATA bindings file and fix 9300-4i4e's GPIO and I2C configuration
SCGCQ00435308 (CSET) - IOP: Memory Coherency not enabled in Detroit
SCGCQ00438969 (ENHREQ) - Update SAS9311-8i IR NVDATA for Channel configuration requirements
SCGCQ00438970 (ENHREQ) - Update SAS9311-4i4e IR NVDATA for Channel configuration requirements
SCGCQ00439473 (NVDATA) - NVDATA for SAS9310-8i with channel requirements
SCGCQ00439502 (NVDATA) - NVDATA for SAS9300-16e with channel requirements
SCGCQ00439510 (NVDATA) - NVDATA for SAS9311-4i with channel requirements

Total Defects Resolved (3)

(SCGCQ00437674)	*Defect 1/3*
HEADLINE:	Default NVDATA for Gen 3 uses wrong SGPIO clock divider
DESC OF CHANGE:	Altered the default NVDATA to account for the new SGPIO frequency in Mfg Page 12.
TO REPRODUCE:	Look at the documentation from Gen 2 to Gen 3's SGPIO frequency. Notice it changed.
ISSUE DESC:	Gen 2 to Gen 3 changed the clock frequency of the SGPIO. The SGPIO clock divider remained the same. This generated a different bus frequency than desired for the default.

(SCGCQ00440212)	*Defect 2/3*
HEADLINE:	Update NVDATA bindings file and fix 9300-4i4e's GPIO and I2C configuration
DESC OF CHANGE:	Updated NVDATA bindings file and fix 9300-4i4e's GPIO and I2C configuration
TO REPRODUCE:	View the files and notice the missing components.
ISSUE DESC:	The NVDATA bindings file was out of data, and the 9300-4i4e board's GPIO and I2C configuration was missing/incorrect.

(SCGCQ00435308 - Port of SCGCQ00432917)	*Defect 3/3*
HEADLINE:	IOP: Memory Coherency not enabled in Detroit
DESC OF CHANGE:	Enable Memory Coherency in FW.
TO REPRODUCE:	Run FW beyond the start of day. Read the proper register in Detroit and observe Memory Coherency was not enabled.
ISSUE DESC:	Memory Coherency feature was not enabled in Detroit.

Total Enhancements Implemented (2)

(SCGCQ00438969)	*Enhancement 1/2*
HEADLINE:	Update SAS9311-8i IR NVDATA for Channel configuration requirements
NEW FUNCTIONALITY:	Updated the Slot:Connector configuration, ensured the Flash Signature Check was Enabled, enabled SGPIO as appropriate and the drive status mappings, updated Mfg Page 9 resources for IR configuration.

(SCGCQ00438970)	*Enhancement 2/2*
HEADLINE:	Update SAS9311-4i4e IR NVDATA for Channel configuration requirements
NEW FUNCTIONALITY:	Updated the Slot:Connector configuration, ensured the Flash Signature Check was Enabled, enabled SGPIO as appropriate and the drive status mappings, updated Mfg Page 9 resources for IR configuration.

Total NVDATA Changes (3)

(SCGCQ00439473)	*NVDATA 1/3*
HEADLINE:	NVDATA for SAS9310-8i with channel requirements
NEW FUNCTIONALITY:	Added channel requirements for Mfg Page 9 Resources, SGPIO configuration (if applicable), and GPIO configuration.

(SCGCQ00439502)	*NVDATA 2/3*
HEADLINE:	NVDATA for SAS9300-16e with channel requirements
NEW FUNCTIONALITY:	Added channel requirements for Mfg Page 9 Resources, SGPIO configuration (if applicable), and GPIO configuration.

(SCGCQ00439510)	*NVDATA 3/3*
HEADLINE:	NVDATA for SAS9311-4i with channel requirements
NEW FUNCTIONALITY:	Added channel requirements for Mfg Page 9 Resources, SGPIO configuration (if applicable), and GPIO configuration.

Change Summary (Defects=2 Enhancements=6 NVDATA=1)

SCGCQ00425888 (CSET) - HwLinkRate in sas phy 0 shows 6G as max link rate and 1.5G as min link rate

SCGCQ00436293 (CSET) - PL: Serdes temperature sensitivity workaround needs to be enabled for B0 chip as well

SCGCQ00435776 (ENHREQ) - Update SAS9300-8e IT NVDATA for Channel configuration requirements

SCGCQ00436396 (ENHREQ) - Update SAS9300-8i IT NVDATA for Channel configuration requirements

SCGCQ00436441 (ENHREQ) - Update SAS9300-4i4e IT NVDATA for Channel configuration requirements

SCGCQ00436442 (ENHREQ) - Update SAS9300-4i IT NVDATA for Channel configuration requirements

SCGCQ00436284 (CSET) - PL: Update RxLosvref value per SE

SCGCQ00436314 (CSET) - Update product ID in the firmware header to Invader family.

SCGCQ00425896 (NVDATA) - NVData: SAS9300-16e updates to enable Flash Signature Check

Total Defects Resolved (2)

(SCGCQ00425888 - Port of SCGCQ00422172)	*Defect 1/2*
HEADLINE:	HwLinkRate in sas phy 0 shows 6G as max link rate and 1.5G as min link rate
DESC OF CHANGE:	Updated the code to reflect max link rate as 12G and min link rate as 3G.
TO REPRODUCE:	Read sas phy page 0
ISSUE DESC:	HwLinkRate in sas phy 0 shows 6G as max link rate and 1.5G as min link rate

(SCGCQ00436293 - Port of SCGCQ00417770)	*Defect 2/2*
HEADLINE:	PL: Serdes temperature sensitivity workaround needs to be enabled for B0 chip as well
DESC OF CHANGE:	Enabled the workaround for both B0 and C0 silicon.
TO REPRODUCE:	Run the firmware on B0 board and firmware will not execute the workaround.
ISSUE DESC:	Serdes temperature sensitivity workaround was not enabled for B0 silicon.

Total Enhancements Implemented (6)

(SCGCQ00435776)	*Enhancement 1/6*
HEADLINE:	Update SAS9300-8e IT NVDATA for Channel configuration requirements
NEW FUNCTIONALITY:	Updated the Slot:Connector configuration, ensured the Flash Signature Check was Enabled, enabled SGPIO as appropriate and the drive status mappings.

(SCGCQ00436396)	*Enhancement 2/6*
HEADLINE:	Update SAS9300-8i IT NVDATA for Channel configuration requirements
NEW FUNCTIONALITY:	Updated the Slot:Connector configuration, ensured the Flash Signature Check was Enabled, enabled SGPIO as appropriate and the drive status mappings.

(SCGCQ00436441)	*Enhancement 3/6*
HEADLINE:	Update SAS9300-4i4e IT NVDATA for Channel configuration requirements
NEW FUNCTIONALITY:	Updated the Slot:Connector configuration, ensured the Flash Signature Check was Enabled, enabled SGPIO as appropriate and the drive status mappings.

(SCGCQ00436442)	*Enhancement 4/6*
HEADLINE:	Update SAS9300-4i IT NVDATA for Channel configuration requirements
NEW FUNCTIONALITY:	Updated the Slot:Connector configuration, ensured the Flash Signature Check was Enabled, enabled SGPIO as appropriate and the drive status mappings.

(SCGCQ00436284 - Port of SCGCQ00415144)	*Enhancement 5/6*
HEADLINE:	PL: Update RxLosvref value per SE
NEW FUNCTIONALITY:	Some phys on cobra fail to link up because the RxLosVref is not optimal. This is a precautionary change as we've never observed the issue before on the controllers.

(SCGCQ00436314 - Port of SCGCQ00415058)	*Enhancement 6/6*
HEADLINE:	Update product ID in the firmware header to Invader family.
NEW FUNCTIONALITY:	Update product ID in the firmware header to Invader family.

Total NVDATA Changes (1)

(SCGCQ00425896)	*NVDATA 1/1*
HEADLINE:	NVData: SAS9300-16e updates to enable Flash Signature Check
NEW FUNCTIONALITY:	Enable the Flash Signature Check feature by flipping bit 3 of SBR Byte 0x46. Also corrected some comments in Manufacturing Page 6.

Defects=0, Enhancements=0 (Version Change Only)